BMA220

Digital, triaxial acceleration sensor

Data sheet

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BMA220 data sheet	
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BMA220

Triaxial ±2g to ±16g acceleration sensor with on-chip motion-triggered interrupt controller

Key features

- Three-axis accelerometer
- Ultra-Small package — Mold package (LGA 12ld), Footprint 2mm x 2mm, height 0.98mm
- Digital interface — SPI (4-wire, 3-wire), I²C, interrupt pin, I/O supply voltage range: 1.6V to 3.6V
- Programmable functionality — Acceleration ranges ±2g/±4g/±8g/±16g, Bandwidth 1kHz . . . 32Hz, Self test
- On-chip interrupt controller — Motion-triggered interrupt-signal generation for
  - orientation recognition
  - any-motion detection
  - tap/double tap sensing
  - low-g/high-g detection

  Stand-alone capability (no microcontroller needed)
- Ultra-low power ASIC — Low current consumption, short wake-up time, advanced features for system power management
- RoHS compliant, halogen-free

Typical applications

- Display profile switching
- Tap/double tap sensing
- Menu scrolling
- Gaming
- Drop detection for warranty logging
- Advanced system power management for mobile applications

General description

The BMA220 is a triaxial, low-g acceleration sensor with digital output for consumer market applications. It allows measurements of acceleration in three perpendicular axes. An evaluation circuitry (ASIC) converts the output of a micromechanical acceleration-sensing structure (MEMS) that works according to the differential capacitance principle.

Package and interface have been defined to match a multitude of hardware requirements. Since the sensor features an ultra-small footprint and a flat package it is ingeniously suited for mobile applications. The sensor offers a variable I/O supply voltage range from 1.6V to 3.6V and can be programmed to optimize functionality, performance and power consumption in customer specific applications. In addition it features an on-chip interrupt controller enabling motion-based applications without use of a microcontroller.

The BMA220 senses tilt, motion and shock vibration in cell phones, handhelds, computer peripherals, man-machine interfaces, virtual reality features and game controllers.

CONTENT

1 Specification

If not stated otherwise, the given values are maximum values over lifetime and full performance temperature and voltage ranges. Min/max. data represent 3-sigma values.

Table 1: Operating conditions, output signal and mechanical characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Units
OPERATING CONDITIONS						
Acceleration Range	g_{FS2g}	switchable via serial digital interface		±2.0		g
	g_{FS4g}			±4.0		g
	g_{FS8g}			±8.0		g
	g_{FS16g}			±16.0		g
Supply Voltage Analog Domain	V_{DDA}		1.62	1.8	1.98	V
Supply Voltage Digital Domain	V_{DDD}		1.62	1.8	1.98	V
Supply Voltage I/O Domain	V_{DDIO}		1.62		3.6	V
Voltage Input Low Level	$V_{IL\ SPI}$	SPI			$0.1*V_{DDIO}$	V
	$V_{IL\ I2C}$	I²C			$0.3*V_{DDIO}$	V
Voltage Input High Level	$V_{IH\ SPI}$	SPI	$0.9*V_{DDIO}$			V
	$V_{IH\ I2C}$	I²C	$0.7*V_{DDIO}$			V
Voltage Output High Level	V_{OH}	SPI & I²C	V_{DDIO}			V
Voltage Output Low Level	$V_{OL\ SPI}$	SPI	GND			V
	$V_{OL\ I2C}$	I²C, $R_P \geq 680\ \Omega$			$0.2*V_{DDIO}$	V
Supply Current in Normal Mode	I_{DD}	Nominal V_{DD} supplies at T_A=25°C		250		µA
Supply current in Low Power Mode	I_{DDsl}	Nominal V_{DD} supplies T_A=25°C, BW = 1kHz sleep dur. > 25ms		< 10		µA
Supply Current in Suspend Mode	I_{DDsd}	Nominal V_{DD} supplies at T_A=25°C			< 1	µA
Wake-Up Time	t_{w_up}	from sleep/suspend mode @1kHz bw			1.2	ms
Start-Up Time	t_{s_up}	POR @1kHz bw		1.5		ms
Operating Temperature	T_A		-40		+85	°C

OUTPUT SIGNAL						
Device resolution	D_{res}	g_{FS2g}		62.5		mg
Sensitivity	S_{2g}	g_{FS2g}, T_A=25°C		16		LSB/g
	S_{4g}	g_{FS4g}, T_A=25°C		8		LSB/g
	S_{8g}	g_{FS8g}, T_A=25°C		4		LSB/g
	S_{16g}	g_{FS16g}, T_A=25°C		2		LSB/g
Sensitivity Temperature Drift	TCS	-40°C ≤ T_A ≤ +85°C		±0.03		%/K
Zero-g Offset	Off	T_A=25°C, V_{DDA}=1.8V, g_{FS2g}		±100		mg
Zero-g Offset Temperature Drift	TCO	-40°C ≤ T_A ≤ +85°C, g_{FS2g}		±2		mg/K
Bandwidth	bw	1st order filter, switchable		32/64/ 125/250/ 500/1000		Hz
Nonlinearity	NL	best fit straight line		±2		%FS
Self Test Response	TSTx	depending on sensitivity/ acceleration range		0.7g*S_x		LSB
	TSTy			2.0g*S_y		LSB
	TSTz			0.6g*S_z		LSB
Output Noise	n_{rms}	rms, Nominal V_{DD} supplies T_A=25°C, BW = 1kHz		2		mg/√Hz
MECHANICAL CHARACTERISTICS						
Cross Axis Sensitivity	$\overline{S}$	relative contribution between 3 axes		2		%
Alignment Error	δ_a	relative to package outline		±0.5		°

2 Absolute maximum ratings

All voltages below are given with respect to GND.

Table 2: Absolute maximum ratings

Parameter	Condition	Min	Max	Units
Voltage at supply pad	V_{DDD} and V_{DDA}	-0.3	2.0	V
	V_{DDIO}	-0.3	4.25	V
Voltage at any logic pad	Non-supply pad	-0.3	V_{DDIO}+0.3	V
Storage temperature range	rel. humidity <=65%	-50	+150	°C
Mechanical shock	duration ≤ 200µs		10,000	g
	duration ≤ 1.0ms		2,000	g
	free fall onto hard surfaces		1.8	m
ESD	HBM, at any pin		2	kV

3 Block diagram

The following figure describes the functionality of the two basic parts of the sensor module, namely mechanical sensor element and evaluating ASIC.

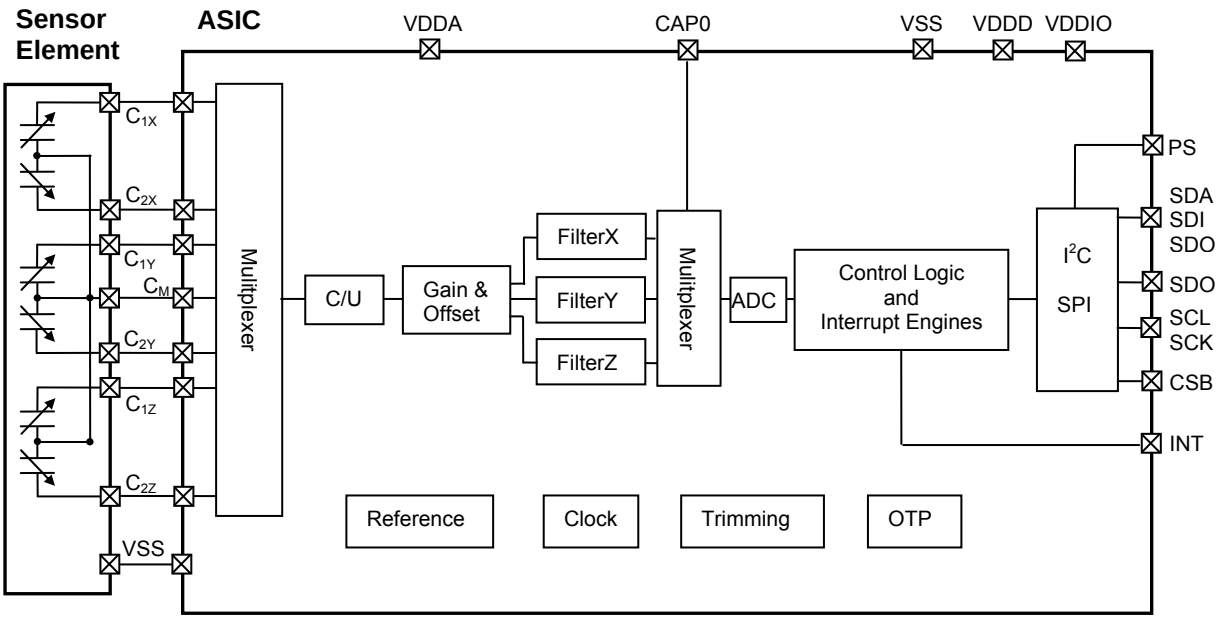


Figure 1: Block diagram BMA220

4 Global memory map

The memory map below shows all externally accessible data registers which are needed to operate BMA220.The left columns show the memory addresses. The columns in the middle depict the content of each register bit. The colors of the bits indicate whether they are read-only, write-only or read- and writable. The memory is volatile so that the writable content has to be re-written after each power-on.
The extended address space greater than 0x19 (SPI) / 0x32 (I^2C) is not shown. These registers are reserved for further Bosch factory testing and trimming.

Register Address (I^2C)	Register Address (SPI)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	default after power-up
0x32	0x19	softreset								0x00
0x30	0x18	suspend								0x00
0x2E	0x17	unused					WDT_TO_en	WDT_TO_sel	SPI3	0x00
0x2C	0x16	reserved								0x00
0x2A	0x15	reserved								0x00
0x28	0x14	reserved								0x00
0x26	0x13	reserved								0x00
0x24	0x12	reserved								0x10
0x22	0x11	unused			sbist_sign	sbist (off,x,y,z)		range[1:0]		0x00
0x20	0x10	serial_high_bw	unused			filt_config[3:0]				0x00
0x1E	0x0F	unused	sleep_en	sleep_dur[2:0]			en_x_channel	en_y_channel	en_z_channel	0x07
0x1C	0x0E	reset_int	lat_int[2:0]			en_low	en_high_x	en_high_y	en_high_z	0x00
0x1A	0x0D	en_data	en_orient	en_slope_x	en_slope_y	en_slope_z	en_tt_x	en_tt_y	en_tt_z	0x00
0x18	0x0C	unused			tt_int	low_int	high_int	data_int	slope_int	0x00
0x16	0x0B	orient_int	orient[2:0]			int_first_x	int_first_y	int_first_z	int_sign	0x00
0x14	0x0A	unused			tip_en	orient_blocking [1:0]		tt_samp[1:0]		0x08
0x12	0x09	orient_ex	slope_filt	slope_th[3:0]				slope_dur[1:0]		0x45
0x10	0x08	tt_filt	tt_th[3:0]				tt_dur[2:0]			0xB5
0xE	0x07	low_hy[1:0]	low_dur[5:0]							0x7F
0xC	0x06	low_th[3:0]				high_th[3:0]				0x4E
0xA	0x05	high_hy[1:0]	high_dur[5:0]							0x7F
0x8	0x04	acc_z<5:0>						0	0	0x00
0x6	0x03	acc_y<5:0>						0	0	0x00
0x4	0x02	acc_x<5:0>						0	0	0x00
0x2	0x01	Revision ID								0x00
0x0	0x00	Chip ID								0xDD

	w/r
	write only
	read only

Figure 2: Memory map

Note: From SPI → I²C use burst address increment in 0x02h steps.

4.1 Control registers

4.1.1 3-wire SPI mode selection

The BMA220 supports both 4-wire and 3-wire SPI. The protocols are exactly the same except for the fact that in 3-wire mode, the SDI pin is also used for data output.
The default mode is 4-wire SPI. If 3-wire SPI should be used, the SPI3 bit in register 0x17 (SPI) must be set to '1'.

4.1.2 Low-power mode configuration

The BMA220 supports a low-power mode. In this low-power mode, the chip wakes up periodically, enables the interrupt controller and goes back to sleep if no interrupt has occurred. The procedure is the following:

1. Wake-up
2. Enable analog front-end and convert acceleration data until the low-pass filters have settled.
3. Enable integrated interrupt controller and evaluate interrupt conditions.
   Once the interrupt conditions have been evaluated and **no** interrupt has occurred, the chip goes back to sleep. If no interrupt is enabled, the acceleration for x-, y- and z-axes are converted once and then the chip goes back to sleep.
4. Sleep for the programmed duration

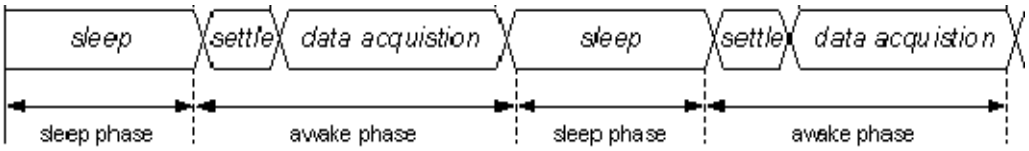


Figure 3: sleep and awake phases

The low-power mode can be enabled by setting the `sleep_en` bit in Reg. 0x0F (SPI) / 0x1E (I^2C). The sleep duration can be configured via the `sleep_dur` bits in Reg 0x0F (SPI) / 0x1E (I^2C).

sleep_dur setting	Sleep Duration
000	2ms
001	10ms
010	25ms
011	50ms
100	100ms
101	500ms
110	1s
111	2s

Table 3: Sleep durations for low-power mode

4.1.3 Low-power mode dimensioning

The power saving that can be achieved depends on the programmed sleep duration and the configured bandwidth. Figure 4 explains the power consumption in relation to the different ASIC states (sleep and awake phases).

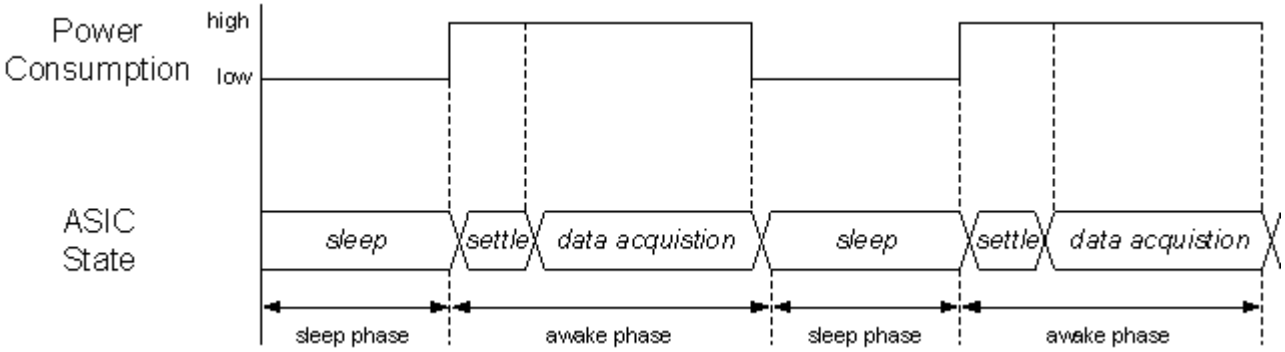


Figure 4: Sleep and awake phase

If a low bandwidth is selected, the time required for filter settling might be the dominating time. Refer to table 2 for the appropriate dimensioning of the attainable current saving.

Filter cut-off	Settling time 2k sampling mode	Settling time 4k sampling mode
32 Hz	16440µs	16690µs
64 Hz	8440µs	8690µs
125 Hz	4440µs	4690µs
250 Hz	2440µs	2690µs
500 Hz	1440µs	1690µs
1000 Hz	940µs	1190µs

Table 4: Approximate awake phase times for 1 data sample

4.1.4 Channel activation / de-activation

In order to optimize further power consumption of the BMA220, data evaluation of individual axes can be deactivated. Per default, all three axes are active. If the user wants to disable one or more axes, the appropriate `en_?_channel` bits at address 0x0F (SPI) / 0x1E (I^2C) must be set to '0'.

4.1.5 Soft-reset

The BMA220 can be put into a soft-reset state by performing a read from the soft-reset address. To bring the chip back into operation, another read must be performed from the same memory address. The reading returns value 0xFF if the system was in soft reset mode; otherwise it returns value 0x00.

Please note that all internal configuration data programmed by the user will be lost.

4.1.6 Suspend mode

The BMA220 can be put into a suspend mode e.g. to easily achieve a power consumption below 1µA by performing a read from the suspend address. To bring the chip back into normal mode operation, another read must be performed from the same memory address. The reading returns value 0xFF if the system was in suspend mode, otherwise it returns value 0x00.

Please note, that during suspend, all analog modules expect for power-on-reset will be disabled. Only reads through the serial interface are supported during suspend.

4.2 Setting registers

4.2.1 Acceleration range and sensitivity setting

The BMA220 has four different range settings for the full scale acceleration range. In dependence of the use case always the lowest full scale range with the maximum resolution should be selected. Please refer to literature to find out, which full scale acceleration range, which sensitivity or which resolution is the ideal one.

This can be configured via the register bits `range`[1:0] at address 0x11 (SPI) / 0x22 (SPI).

The following table shows the range bits with corresponding scale and resolution.

range[1:0]	Full Scale	Sensitivity	Resolution	Example use case
'00'	±2g	16 LSB / g	62.5mg / LSB	Orientation recognition
'01'	±4g	8 LSB / g	125mg / LSB	Gaming
'10'	±8g	4 LSB / g	0.25g / LSB	
'11'	±16g	2 LSB / g	0.5g / LSB	Shock vibration detection

Table 5: Acceleration resolution

4.2.2 Filter and bandwidth configuration

The BMA220 has a digital filter that can be configured by setting the corresponding register bits `filter_config[3:0]` at address 0x10 (SPI) / 0x20 (I^2C). For compatibility reasons the settings are defined based on BMA120. To always ensure an ideal cut off frequency of the filter the BMA220 is adjusting the sample rate automatically.

filter_config[3:0]	0x5	0x4	0x3	0x2	0x1	0x0
digital filter cut-off frequency	32Hz	64Hz	125Hz	250Hz	500Hz	1kHz

Table 6: Digital filter configuration

The internal SC-filter has a fix cut-off frequency at 1 KHz. In addition to the internal SC-filter a digital filter is available which is providing a filtered and an unfiltered data stream for all of the 3 axes of acceleration.

If application specific reasons require a bandwidth configuration <32Hz, please contact your Bosch Sensortec representative.

4.3 Data registers

4.3.1 Acceleration data read-out

The acceleration data can be read-out through addresses 0x02 (SPI) / 0x04 (I^2C) through 0x04 (SPI) / 0x08 (I^2C). The acceleration data is in 2's complement according to the table below.

An efficient way to read out the acceleration data in I²C or SPI mode is the burst-accesses. During such an access, the BMA220 automatically increments the read address after each byte. By using this kind of access, the data transferred over the I²C bus can be reduced by up to 50%.

Decimal value	Acceleration (in 2g range mode)
+ 31	+ 2g
…	…
0	0g
…	…
-32	- 2.06g

Table 7: Acceleration register content

Per default, the bandwidth of the data being read-out is limited by the internal low-pass filters according to the filter configuration. However, it is possible to read-out data only 1st order filtered (1 kHz) even though the internal filters are configured differently.

The reason for this feature is that the interrupt controller may operate on low-bandwidth data while the external master still needs to operate on high-bandwidth data.

Unfiltered (1kHz high-bandwidth) data can be read-out through the serial interface when the `serial_high_bw` bit is set to '1'. Per default, filtered data is read-out through the serial interface.

4.3.2 Chip / revision ID

The chip ID and the revision ID can be read-out through addresses 0x00 (SPI & I^2C) and 0x01 (SPI) / 0x02 (I^2C).

Chip ID	Revision ID
0xDD	0x00

Table 8: Chip and revision ID

4.4 Interrupt control registers

The BMA220 features a programmable interrupt controller that directly supports common mobile applications like tap sensing detection, orientation recognition and any-motion detection.

Supported types of interrupts:

- Any-motion (slope) detection
- Tap/double-tap sensing
- Orientation recognition
- Low-g detection
- High-g detection
- Data-ready interrupt

The configuration and status register bits of all interrupt engines and the exact interrupt functionality are given in chapter 5.

5 Interrupt controller

The BMA220 integrates a programmable interrupt controller. It can be configured via SPI/I^2C to monitor individual axes (X-, Y- and Z-axis) and check whether certain conditions apply (e.g. the acceleration on one axis exceeds a certain threshold). The interrupt controller of the BMA220 is capable of checking for certain conditions simultaneously.

If at least one of the configured conditions applies, an interrupt (logic '1') is issued through the INT pin of the sensor. More details about the triggering condition (e.g. the type of the interrupt or the axis that triggered the interrupt) are saved in internal status registers and can be read out through the digital interface.

It is recommended to reset the interrupt controller by setting reset_int to '1' when the interrupt settings has been set or changed.

5.1 Latched vs. non-latched modes

The interrupt controller can be used in two modes

- Latched mode: Once one of the configured interrupt conditions applies, the INT pin is asserted and must be reset by the external master through the digital interface.
- Non-Latched mode: The interrupt controller clears the INT signal once the interrupt condition no longer applies.

The interrupt output can be programmed by *lat_int[2:0]* to be either unlatched ('000') or latched permanently ('111') or have the latch time of 0.25s('001')/0.5s('010')/1s('011')/2s('100')/4s ('101')/8s('110'). The setting of these bits applies to all types of interrupts.

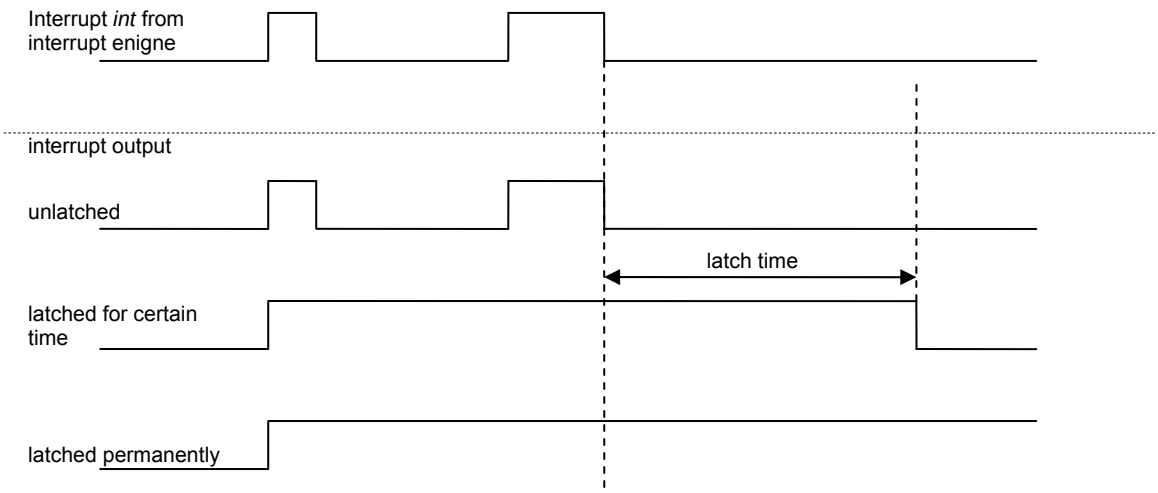


Figure 5: Interrupt output

5.2 Supported types of interrupts

The following interrupt modes are provided by the BMA220.

- Any-motion (slope) detection
- Tap/double-tap sensing
- Orientation recognition
- Low-g detection
- High-g detection
- Data-ready interrupt

5.3 Power-saving modes

In order to reduce power consumption of the sensor itself, the BMA220 supports a low-power mode in which the ASIC wakes up periodically, checks whether any of the configured interrupt conditions apply and then either goes back to sleep (no interrupt) or stays awake (interrupt).

The BMA220's PMU (power management unit) controls the transitions from the 'awake state' into the 'sleep state' and vice versa.

In normal mode, the interrupt controller is permanently turned on to continuously process the incoming data. In low-power mode, the interrupt controller will be turned on by the PMU once the chip has fully woken up. The time it takes before the sensor can go back to sleep is determined by the active interrupt engines. Once all active engines indicate that no interrupt condition applies, the PMU will switch the sensor back into sleep state (please refer to section 0 for more details).

Furthermore the applied interrupt condition can be used not only to enable the low-power mode of the sensor itself but for the whole system. This enables a dramatically reduced power consumption of the whole system. The result is an extended operation and stand-by time e.g. of mobile devices in an order of magnitude.

5.4 Any-motion (slope) detection

The any-motion detection uses the slope between two successive acceleration signals to detect changes in motion. It generates an interrupt when a preset threshold *slope_th* is exceeded. The threshold can be configured between 0 and the maximum acceleration value corresponding to the selected measurement range. The time difference between the successive acceleration signals depends on the bandwidth of the configurable low pass filter and corresponds roughly to 1/(2*bandwidth) (∆t=1/(2*bw)).

In order to suppress failure signals, the interrupt is only generated if a certain number *slope_dur* of consecutive slope data points is above the slope threshold *slope_th*.

If the same number of data points falls below the threshold, the interrupt is reset.

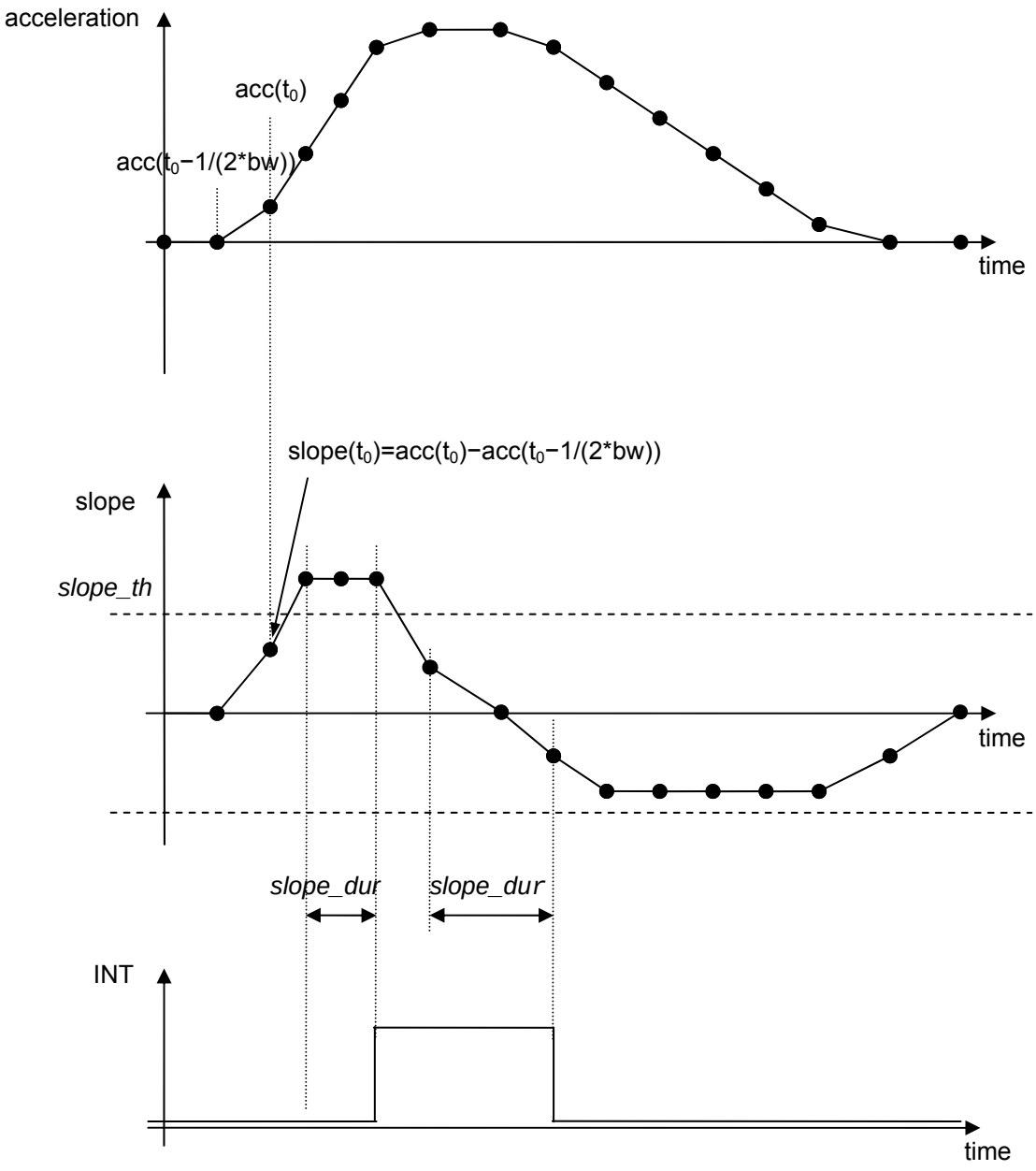
The criteria for any-motion detection are fulfilled and the slope interrupt is generated if any of the enabled channels exceeds the threshold *slope_th* for *slope_dur* consecutive times. As soon as all the enabled channels fall or stay below this threshold for *slope_dur* consecutive times the interrupt is reset unless interrupt signal is latched.

The any-motion interrupt logic sends out the signals of the axis that has triggered the interrupt (*slope_first_x*, *slope_first_y*, *slope_first_z*) and the signal of motion direction (*slope_sign*).

When serial interface is active, any-motion detection logic is enabled if any of the any-motion enable register bits is set. To disable the any-motion interrupt, clear all the axis enable bits.

In the dedicated wake-up mode (0), all three axes are enabled for any-motion detection whether the individual axis enable bits are set or not.

Figure 6: Any-motion (slope) interrupt detection



The following table shows the signals used in any-motion detection. After reset, a default value will be assigned to each register.

Name	Register Address (SPI) *	Description	Number of bits	Reset-value
en_slope_x en_slope_y en_slope_z	0x0D.5 0x0D.4 0x0D.3	enable slope detection on x-axis enable slope detection on y-axis enable slope detection on z-axis	3	“000”
slope_th	0x09[5:2]	define the threshold level of the slope 1 LSB threshold is 1 LSB of acc_data	SLOPE_TH_NUM 4	SLOPE_TH_INIT (“0001”)
slope_dur	0x09[1:0]	define the number of consecutive slope data points above *slope_th* which are required to set the interrupt (“00” = 1,”01” = 2,”10” = 3, “11” = 4)	SLOPE_DUR_NUM 2	SLOPE_DUR_INIT (“01”)
slope_filt	0x09.6	defines whether filtered or unfiltered acceleration data should be used (evaluated) (‘0’=unfiltered, ‘1’=filtered)	1	‘1’
slope_int	0x0C.0	whether slope interrupt has been triggered	1	‘0’
slope_first_x slope_first_y slope_first_z		whether x-axis has triggered the interrupt (0=no, 1=yes) whether y-axis has triggered the interrupt (0=no, 1=yes) whether z-axis has triggered the interrupt (0=no, 1=yes)	3	“000”
slope_sign		global register bit for all interrupts define the slope sign of the triggering signal (0=positive slope, 1=negative slope)	1	‘0’

* For determining the corresponding I^2C register address, please refer to figure 2 in chapter 4 (memory map)

Table 9: Control and status register for any motion detection

5.5 Tap sensing

Tap sensing has the same functionality as a common laptop touch-pad. If 2 taps occur within a short time, a pre-defined action will be performed by the system. If time between 2 taps is too long or too short no action happens.

When the serial interface is activated, tap sensing is enabled if any of the tap sensing enable register bits are set (*en_tt_x, en_tt_y, en_tt_z*). To disable the tap sensing interrupt, clear all the axis enable bits.

When the preset threshold *tt_th* is exceeded, a tap-shock is detected. The tap sensing interrupt is generated only when a second tap is detected within a specified period of time.

The slope between two successive acceleration data has to exceed *tt_th* to detect a tap-shock. The time difference between the two successive acceleration values depends on the bandwidth of the low pass filter. It roughly corresponds to 1/(2*bandwidth).

The time delay *tt_dur* between two taps is typically between 12,5ms and 500ms. The threshold is typically between 0.7g and 1.5g in 2g measurement range. Due to different coupling between sensor and device shell (housing) and different measurement ranges of the sensor these parameters are configurable.

The criteria for tap sensing are fulfilled and the interrupt is generated if the second tap occurs after *tap_quiet* and within *tt_dur*. The tap sensing direction is determined by the 1st tap. During *tt_quiet* period (30ms) no taps should occur. If a tap occurs during *tap_quiet* period it will be connoted as new tap.

The slope detection interrupt logic stores the direction of the (first) tap-shock in a status register. This register will be locked for *tap_shock*=50ms in order to prevent other slopes to overwrite this information.

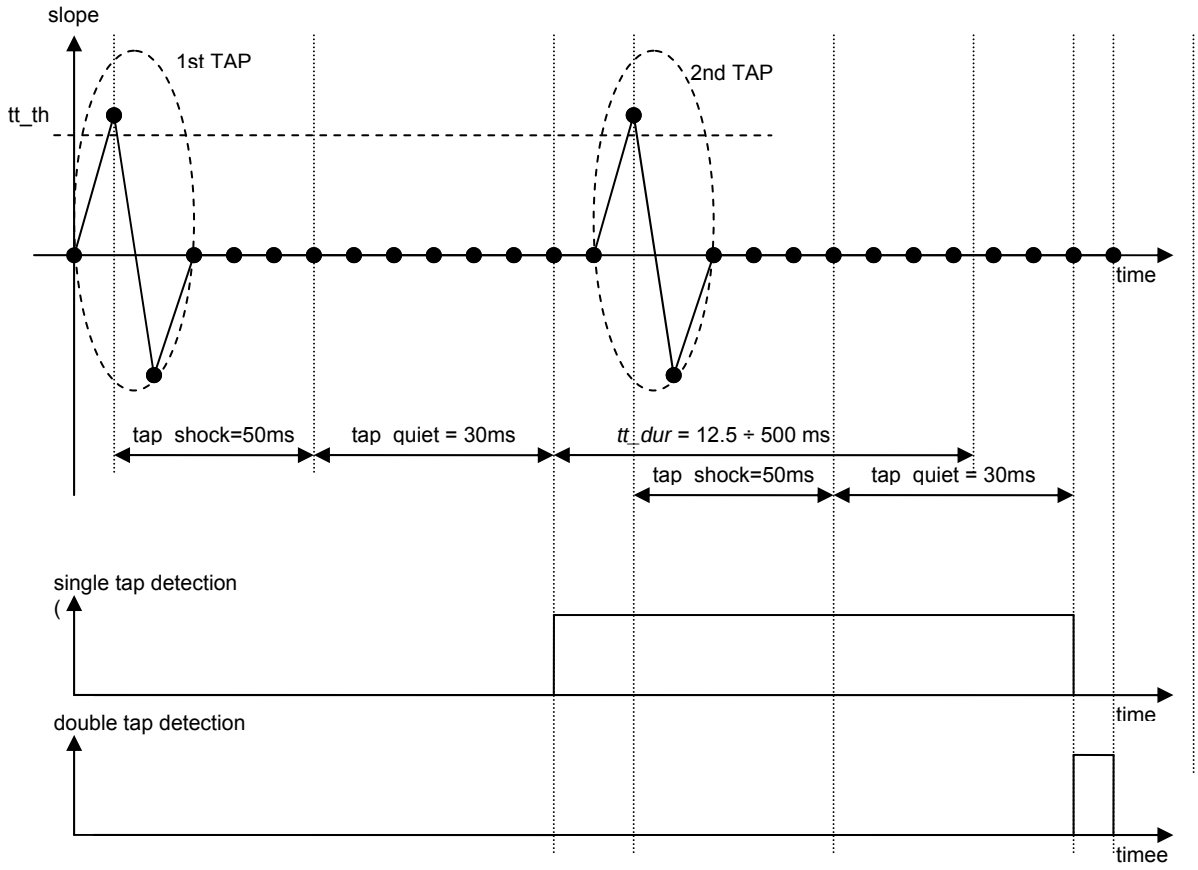
When a tap sensing interrupt is triggered, the signals of the axis that has triggered the interrupt (*tt_first_x*, *tt_first_y*, *tt_first_z*) and the signal of motion direction (*tt_sign*) are stored in the corresponding registers.

The axis on which the biggest slope occurs will trigger the first tap. The second tap will be triggered by any axis (not necessarily same as the first tap).

The register *tap_en* defines whether single tap or double tap shall be detected.

In dedicated tap sensing mode, all three axes are enabled for double tap sensing detection.

Figure 7: Tap sensing interrupt detection



When a tap-sensing interrupt is triggered, the following details can be read from the corresponding registers: the axis that has triggered the interrupt (*tt_first_x*, *tt_first_y*, *tt_first_z*) and the motion direction of the triggering acceleration signal (*tt_sign*).

Name	Register Address (SPI) *	Description	Number of bits	Reset-value
en_tt_x en_tt_y en_tt_z	0x0D.2 0x0D.1 0x0D.0	enable tap sensing detection on x-axis enable tap sensing detection on y-axis enable tap sensing detection on z-axis	3	“000”
tt_th	0x08[6:3]	define the threshold level of the tap sensing slope 1 LSB is 2*(LSB of acc_data)	TT_TH_NUM 4	TT_TH_INIT “0110”
tt_dur	0x08[2:0]	define the maximum delay of the second tap after the shock suppression (50, 105, 150, 219, 250, 375, 500, 700)ms	TT_DUR_NUM 3	TT_DUR_INIT “101”
tt_filt	0x08.7	defines whether filtered or unfiltered acceleration data should be used (evaluated) (‘0’=unfiltered, ‘1’=filtered)	1	‘1’
tip_en	0x0A.4	whether tap or double-tap shall be detected (0= double tap, 1=tap)	1	‘0’
tt_int	0x0C.4	whether tap sensing interrupt has been triggered (0=no, 1=yes)	1	‘0’
tt_samp	0x0A[1:0]	number of data to be sampled after wake-up ‘00’ => 2 data ‘01’ => 4 data ‘10’ => 8 data ‘11’ => 16 data	2	‘00’
tt_first_x tt_first_y tt_first_z		whether x-axis has triggered the interrupt (0=no, 1=yes) whether y-axis has triggered the interrupt (0=no, 1=yes) whether z-axis has triggered the interrupt (0=no, 1=yes)	3	“000”
tt_sign		give the slope sign of the triggering signal (0=positive, 1=negative)	1	‘0’

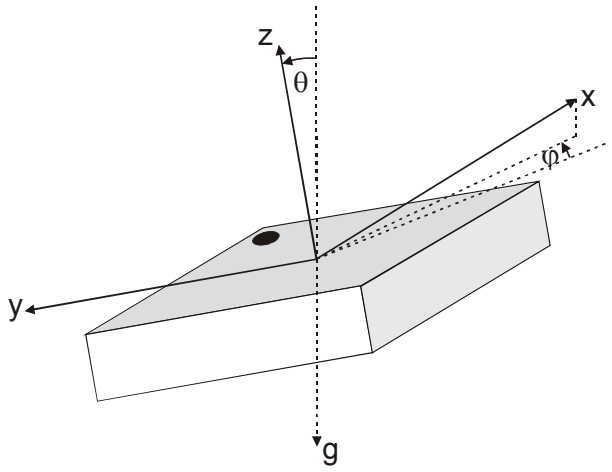
* For determining the corresponding I^2C register address, please refer to figure 2 in chapter 4 (memory map)

Table 10: Control and status register for tap sensing

5.6 Orientation recognition

The orientation recognition feature informs on an orientation change of the sensor with respect to the gravitational field vector g. The measured acceleration vector components with respect to the gravitational field look as follows.

Figure 8: Definition of acceleration-vector components



[with respect to graviational field vector g (black dot = pin 1 identifier)]

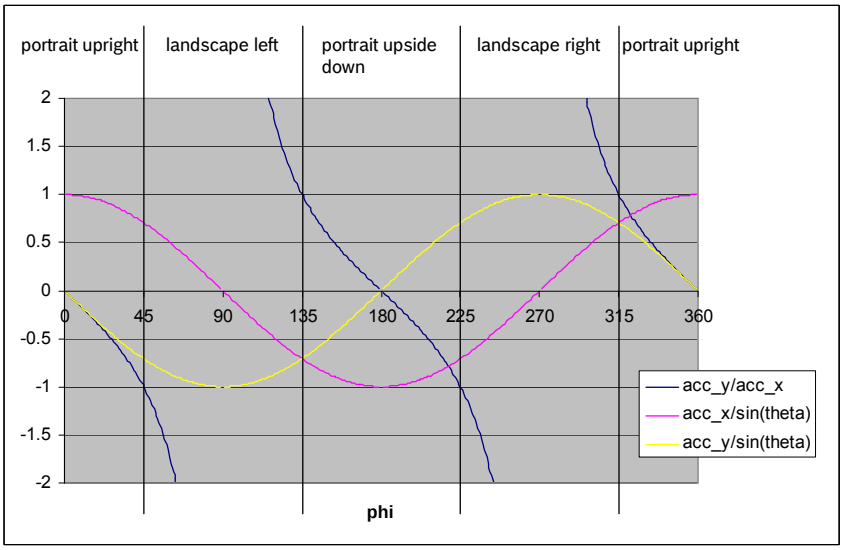
$acc\_x = 1g \cdot \sin\theta \cdot \cos\varphi$
$acc\_y = -1g \cdot \sin\theta \cdot \sin\varphi$
$acc\_z = 1g \cdot \cos\theta$
$\rightarrow acc\_y/acc\_x = -\tan\varphi$

The output register is called *orient* and defined in the following way:

‘0xx’ upward looking (z>0):
- ‘000’ portrait upright (315°<φ<45°) → |acc_y/acc_x|<1 && acc_x>0
- ‘001’ portrait upside down (135°<φ<225°) → |acc_y/acc_x|<1 && acc_x<0
- ‘010’ landscape left (45°<φ<135°) → |acc_y/acc_x|>1 && acc_y<0
- ‘011’ landscape right (225°<φ<315°) → |acc_y/acc_x|>1 && acc_y>0

‘1xx’ downward looking (z<0), xx as before

Figure 9: Orientation definition and interrupt thresholds with respect to the angle phi φ



The criteria for portrait/landscape switching is fulfilled and the interrupt is generated when the threshold |acc_y/acc_x|=1 is crossed (i.e. 45°, 135°, 225°, 315°). As soon as the interrupt is set, no new interrupt is generated within the hysteresis level of 0.66<|acc_y/acc_x|<1.66 corresponding to a hysteresis interval of ±13% around the threshold.

It is possible to block the orientation detection depending on certain conditions (no orientation interrupt will be triggered). This orientation interrupt blocking feature is configurable via the *orient_blocking*[1:0] bits in the following manner:

- '00' → interrupt blocking is completely disabled
- '01' → no interrupt is generated, when |z|>0.9g OR |x|+|y| < 0.4g OR when the slopes of the acceleration data exceeds 0.2g (sample-to-sample).
- '10' → no interrupt is generated, when |z|>0.9g OR |x|+|y| < 0.4g OR while the slopes of the acceleration data exceeds 0.3g (sample-to-sample).
- '11' → no interrupt is generated, when |z|>0.9g OR |x|+|y| < 0.4g OR while the slopes of the acceleration data exceeds 0.4g (sample-to-sample).

For all states where interrupt blocking through slope detection is used, the interrupt should be re-enabled after the slope has been below the threshold for 3 times in a row.

For all states where interrupt blocking is enabled, in order to trigger the interrupt, the orientation should remain the same (stable) until the timer runs out (for ~100ms). The timer starts to count when orientation changes between two consecutive samples. If the orientation changes while timer is still counting, the timer is restarted.

The criteria for switching from upward to downward looking fulfilled and the interrupt is generated when the threshold z=0g is crossed. As soon as the interrupt is set, no new interrupt is generated within the hysteresis level of -0.4g<z<0.4g (i.e. ±25° tilt around vertical position).

The given specification is valid for an upright mounted PCB. In order to enable also horizontal mounting, x and z axis can be exchanged via the register *orient_ex*. The x-, y-, z-axis will keep right-hand principle after the exchange.

When serial interface is active, orientation detection is enabled if the enable bit *en_orient* is set. To disable the orientation interrupt, clear the enable bit.

When the dedicated orientation mode is active, the orientation is given by certain output pins corresponding to the above-given definition of the *orient* register. For details on the output pins see section 0.

In case the orientation interrupt condition has been satisfied and interrupt is not latched, *int* signal is asserted for one data sampling period unless no-reset condition applies.

Name	**Register Address (SPI) ***	**Description**	**Number of bits**	**Reset-value**
orient_ex	0x09.7	exchange x- and z-axis in algorithm, i.e x or z is relevant axis for upward/downward looking recognition (0=z, 1=x)	1	‘0’
Orient	0x0B[6:4]	give the orientation of the sensor with respect to the gravitational force	3	ORIENT_INIT ‘000’
orient_int	0x0B.7	whether orientation interrupt has been triggered (0=no, 1=yes)	1	‘0’
en_orient	0x0D.6	enable signal for orientation detection	1	‘0’
orient_blocking	0x0A	Enable/configure orientation interrupt disable criteria. ‘00’ -> no slope, no wait ‘01’ -> no slope, wait-only (~100ms) ‘10’ -> wait 100ms + |z|-criteria, |x|+|y|-criteria and <0.2g slope ‘11’ -> wait 100ms + |z|-criteria, |x|+|y|-criteria and <0.4g slope	2	‘10’

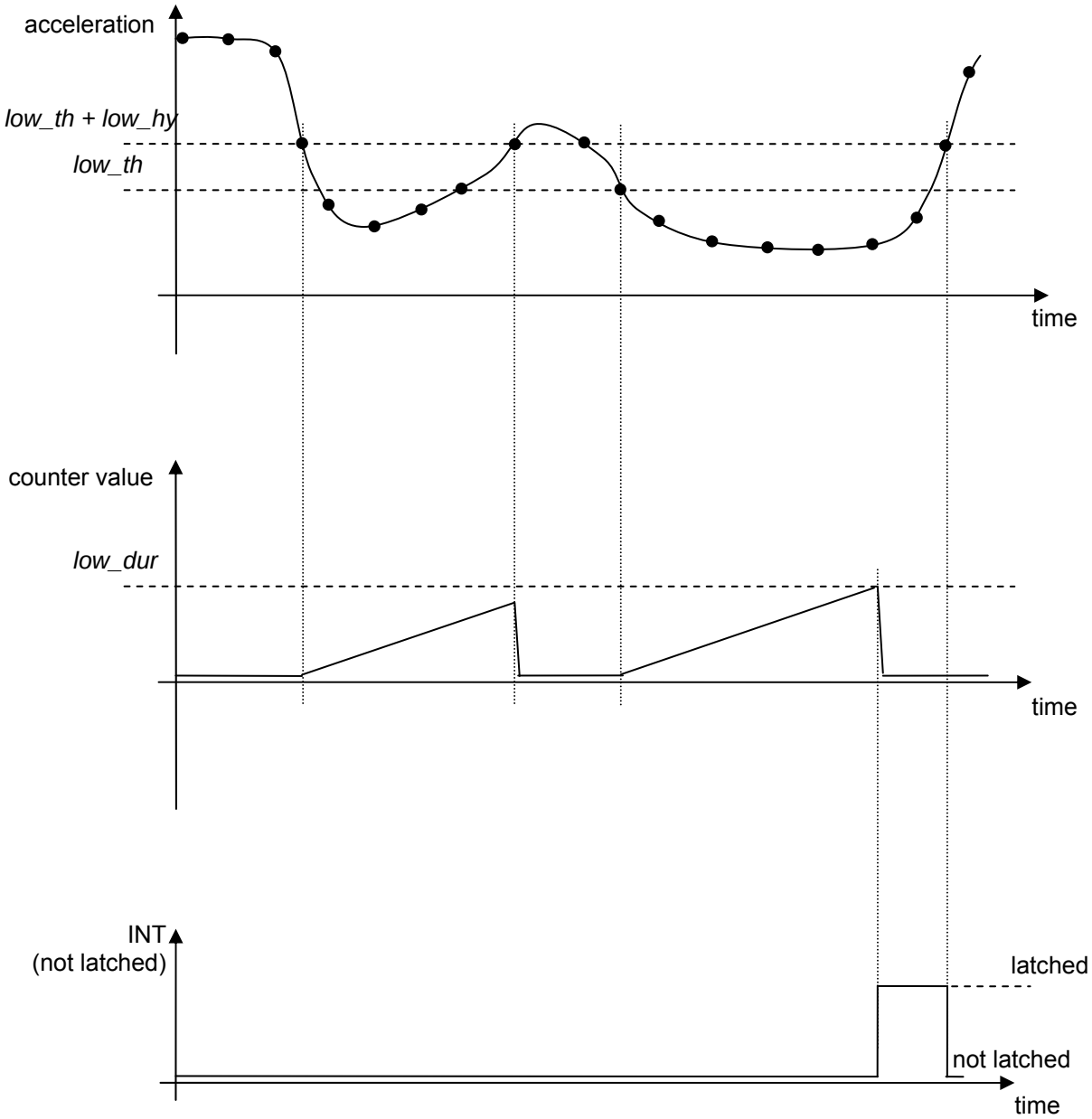
* For determining the corresponding I^2C register address, please refer to figure 2 in chapter 4 (memory map)

Table 11: Control and status register for orientation recognition

5.7 Low-g detection

For freefall detection, the absolute values of the acceleration data of all axes are observed (global criteria). A low-g situation is likely to occur when all axes fall below a lower threshold *low_th*. The interrupt will be generated if the measured acceleration falls below the threshold and stays below the hysteresis level *low_th+low_hy* for a minimum number of data points (*low_dur*). Thus, the duration of a released interrupt is depending on the data sampling rate which is related to the bandwidth.

Figure 10: Low-g interrupt detection



Name	Register Address (SPI) *	Description	Number of bits	Reset-value
Low_th	0x06[7:4]	define the low-g threshold level 1 LSB is 2*(LSB of acc_data)	LOW_TH_NUM 4	LOW_TH_INIT “0100”
Low_hy	0x07[7:6]	define the low-g hysteresis level 1 LSB is 2*(LSB of acc_data)	LOW_HY_NUM 2	LOW_HY_INIT “01”
low_dur	0x07[5:0]	define the number of measured data which has to be lower than *low_th+low_hy* to set the interrupt (max. 64)	LOW_DUR_NUM 6	LOW_DUR_INIT “111111” (3F)
en_low	0x0E.3	enable signal for low-g detection	1	‘0’
low_int	0x0C.3	whether low-g interrupt has been triggered (0=no, 1=yes)	1	‘0’

* For determining the corresponding I^2C register address, please refer to figure 2 in chapter 4 (memory map)

Table 12: Control and status register for low g detection

5.8 High-g detection

For indicating high-g events, an upper threshold can be programmed. The threshold *high_th*, the hysteresis *high_hy* and the duration *high_dur* are defined analogously to the low-g interrupt. The interrupt is generated if one of the three channels exceeds the threshold *hight_th* and does not fall below hysteresis level *high_th-high_hy* for minimum number of data points (*high_dur*).

When the high-g interrupt is triggered, the signals of the axis that has triggered the interrupt (*high_first_x*, *high_first_y*, *high_first_z*) and the signal of motion direction (*high_sign*) will be stored in the corresponding status registers.

Name	**Register address (SPI) ***	**Description**	**Number of bits**	**Reset-value**
high_th	0x06[3:0]	define the high-g threshold level 1 LSB is 2*(LSB of acc_data)	HIGH_TH_NUM 4	HIGH_TH_INIT “1110”
high_hy	0x05[7:6]	define the high-g hysteresis level 1 LSB is 2*(LSB of acc_data)	HIGH_HY_NUM 2	HIGH_HY_INIT “01”
high_dur	0x05[5:0]	define the number of measured signals which has to be higher than *high_th+high_hy* to set the interrupt (max. 64)	HIGH_DUR_NUM 6	HIGH_DUR_INIT “011111” (3F)
en_high_x en_high_y en_high_z	0x0E.2 0x0E.1 0x0E.0	enable high-g detection on x-axis (0=disabled, 1=enabled) enable high-g detection on x-axis (0=disabled, 1=enabled) enable high-g detection on x-axis (0=disabled, 1=enabled)	3	“000”
high_int	0x0C.2	whether high-g interrupt has been triggered (0=no, 1=yes)	1	‘0’
high_first_x high_first_y high_first_z		whether x-axis has triggered the interrupt (0=no, 1=yes) whether y-axis has triggered the interrupt (0=no, 1=yes) whether z-axis has triggered the interrupt (0=no, 1=yes)	3	“000”
high_sign		give the slope sign of the triggering signal (0=positive, 1=negative)	1	‘0’

***** For determining the corresponding I^2C register address, please refer to figure 2 in chapter 4 (memory map)

Table 13: Control and status register for high g detection

5.9 Data ready detection

This interrupt provides the possibility of synchronously reading out data from the BMA220 without missing a single data point. The data update detection monitors the *data_update* signals for all axes. It generates an interrupt as soon as the acceleration values for all enabled axes have been updated. The signal *en_x_channel*, *en_y_channel* and *en_z_channel* are the enable signals for the data conversion from each axis accordingly. The three enable signals can be configured by users (see section 0). For example, if all three axes are enabled, the interrupt is generated after updated signals for x-, y-, and z-axes have been detected.

When data ready detection is activated, all other interrupts are not propagated to the INT pin. However their status can still be obtained from the appropriate registers.

When the data-ready interrupt is not latched, the interrupt is cleared automatically after ~150µs.

Name	Description	Number of bits	Reset-value
en_data	enable signal for data-ready detection	1	'0'
data_int	whether data-ready interrupt has been triggered (0=no, 1=yes)	1	'0'

Table 14: Control and status register for low g detection

6 Operation modes

Depending on the configuration the BMA220 is able to operate in two different types of modes

- General mode: A serial interface is active (SPI or I^2C). Several interrupt engines may be activated in parallel. Through the serial interface, the external master (e.g. µC) can configure the interrupts of the BMA220 and read-out information about the current interrupt status.

- Dedicated mode: No serial interface is present. Internal default settings for all interrupt engines must be used. In these modes, only one interrupt engine can be active at a time. Currently, dedicated modes exist for the orientation interrupt, the tap sensing interrupt and the any-motion interrupt. The dedicated mode allows the sensor to be operated as a stand alone device, e.g. without any µC and without dealing with any acceleration data. So, in a very user friendly and convenient way taps/double-taps, orientation changes and wake-ups can be processed by a simple µC-less system.

A flow chart of the different modes is depicted in figure 11:

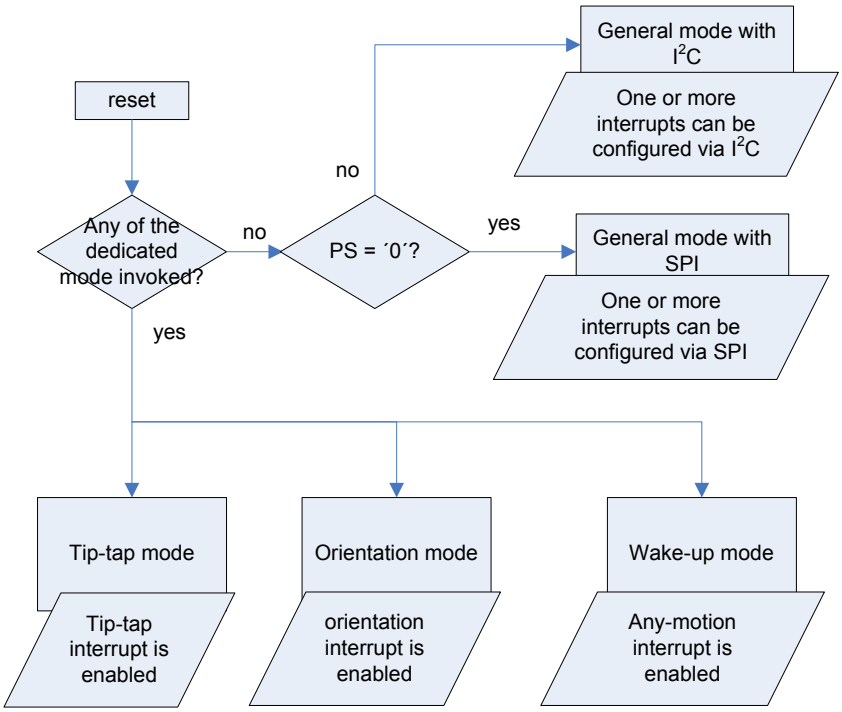


Figure 11: Interrupt modes

Mode	PS	SCK	INT
SPI	0		
I²C	1		
Dedicated orientation	Z	0	
Dedicated tap sensing	Z	1	0
Dedicated wake-up	Z	1	1

Table 15: Mode selection

Please note that the PS must be connected to the appropriate supply (or left floating) at start-up (reset). The “Z-detection” circuit will be turned off when a stable value at the PS pin has been detected. Thus, the dedicated modes can be only activated after reset. Switching from one interface mode to another during operation may work but can not be guaranteed by the ASIC. The reason for this limitation is that the circuitry for z-detection consumes several µA.

For debugging/test purposes, turning-off the z-detection circuitry can be suppressed by setting the `comp_always_on` bit within the OTP memory range.

Pin #		2	1	10	12	5	11	6	3	4	7	8, 9
Mode		**SDI**	**SDO**	**CSB**	**SCK**	**INT**	**PS**	**CAP0**	**V_{DDIO}**	**V_{DDD}**	**V_{DDA}**	**GND**
SPI 4 wire		SDI	SDO	CSB	SCK	INT	GND	NC	V_{DDIO}	V_{DDD}	V_{DDA}	GND
SPI 3 wire		SDA	NC	CSB	SCK	INT	GND	NC	V_{DDIO}	V_{DDD}	V_{DDA}	GND
I²C		SDA	NC	I²C lsb_invert	SCL	INT	V_{DDIO}	NC	V_{DDIO}	V_{DDD}	V_{DDA}	GND
Dedicated mode (w/o µC); stand-alone	Orientation	ORIENT_0	ORIENT_1	sleep_time	GND	ORIENT_2	NC	NC	V_{DDIO}	V_{DDD}	V_{DDA}	GND
	Tap sensing	SINGLE_TAP	DOUBLE_TAP	sleep on	V_{DDIO}	GND	NC	NC	V_{DDIO}	V_{DDD}	V_{DDA}	GND
	Wake-up	WAKE_UP_INT	NC	sleep_time	V_{DDIO}	VDDIO	NC	NC	V_{DDIO}	V_{DDD}	V_{DDA}	GND

Table 16: Pin assignments for all operation modes

6.1 Dedicated Modes (µC-less / stand alone)

After reset (POR, soft-reset or reset pin) the system monitors the pin PS (Protocol Select). If the pin is unconnected, an internal module detects the floating state and enables one of the dedicated modes depending on the other select pins (SCK, INT).

There are three different dedicated modes:

- Orientation detection mode: only orientation interrupt detection is enabled.
- Tap/double-tap detection mode: only tap sensing interrupt detection is enabled.
- Wake-up detection mode: only wake-up interrupt detection is enabled

In dedicated mode, the interrupt engine uses default settings for all configuration registers. Those default settings are loaded after reset and are listed in section 0. Changing the default

configuration of the registers is not possible while the chip is in the dedicated mode.
Currently, in orientation and wake-up mode, the user can select between two different sleep durations via the CSB pin:

Dedicated Mode	CSB	Sleep duration
Dedicated orientation	0	100ms
	1	1s
Dedicated wake-up	0	10ms
	1	500ms
Dedicated tap-sensing	0	No sleep
	1	2ms

Table 17: Sleep durations for dedicated modes

Dedicated Mode	Bandwidth
Dedicated orientation	32Hz
Dedicated wake-up	16Hz
Dedicated tap-sensing	1kHz

Table 18: Filter bandwidths for dedicated modes

6.2 Digital interface modes

The BMA220 supports two different digital interfaces (SPI and I²C). The currently active general interface is determined by the primary input PS. The configuration of interrupt engines is fully customizable via the defined digital interface.

- SPI Active Mode: The SPI interface is enabled while PS is externally connected to GND (logic '0' detected).
- I^2C Active Mode: The I²C interface is enabled while PS is externally connected to VDD (logic '1' detected).

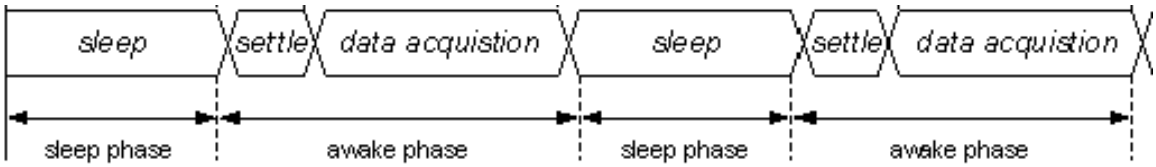
6.3 Low-power mode and suspend mode

The BMA220 is optimized for low power consumption. Therefore, the BMA220 supports two energy saving modes: a *suspend* mode and a *low-power mode*.

During normal mode operation, all analog modules are held powered-up and the clock for all digital modules is active. During *low-power mode*, the analog modules in the rate channel are held powered down and the clock of the digital rate, filter and trimming modules is gated. The average typical current consumption during sleep phase ($i_{low\_power\_mode}$) can be estimated by the following equation:

First approximation: $i_{sleep} = i_{suspend}$

Ø typ. $$i_{low\_power\_mode} \approx \frac{t_{sleep} \cdot i_{suspend} + t_{active} \cdot i_{active}}{t_{sleep} + t_{awake}}$$



For sleep phase time setting (t_{sleep}) refer to chapter 4.1.2 table 3.
For approximate awake phase time (t_{awake}) refer to chapter 4.1.3 table 4.
For current consumption in normal mode (i_{active}) refer to chapter 1.
For current consumption in suspend mode ($i_{suspend}$) refer to chapter 1.

Example:

Bandwidth (BW) = 1kHz, nominal supplies

- resulting awake phase for 1st data sample (t_{awake}) = 1190µs = 1.190ms
- resulting sleep time (t_{sleep}) = 50 ms

Ø typ. $$i_{low\_power\_mode} \approx \frac{t_{sleep} \cdot i_{suspend} + t_{active} \cdot i_{active}}{t_{sleep} + t_{awake}} \approx \frac{50ms \cdot 1\mu A + 1{,}190ms \cdot 250\mu A}{50ms + 1{,}190ms} \approx 6{,}8\mu A$$

6.4 Mode transition via interface

While the SPI or the I²C interfaces are active, transitions between the individual modes can be triggered via register accesses.

1. **Low-power:** The BMA220 switches into low-power mode after *setting* the `sleep_en` register depicted in the memory map. While the BAA220 is in low-power mode, a period wake-up is performed (please refer to section 0). Normal mode operation is resumed after *writing a '0'* to the `sleep_en` register. The sleep register is user accessible.

2. **Suspend:** The BMA220 is put into suspend mode by *reading* from the suspend address. A subsequent read switches back to the previous state. Concluding, a read from the suspend address toggles the suspend register.

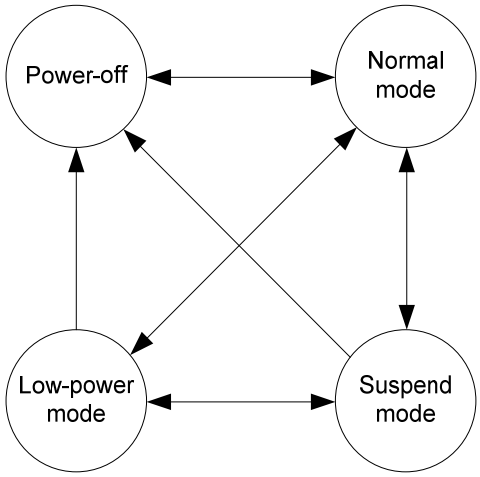


Figure 12: Energy saving mode transitions

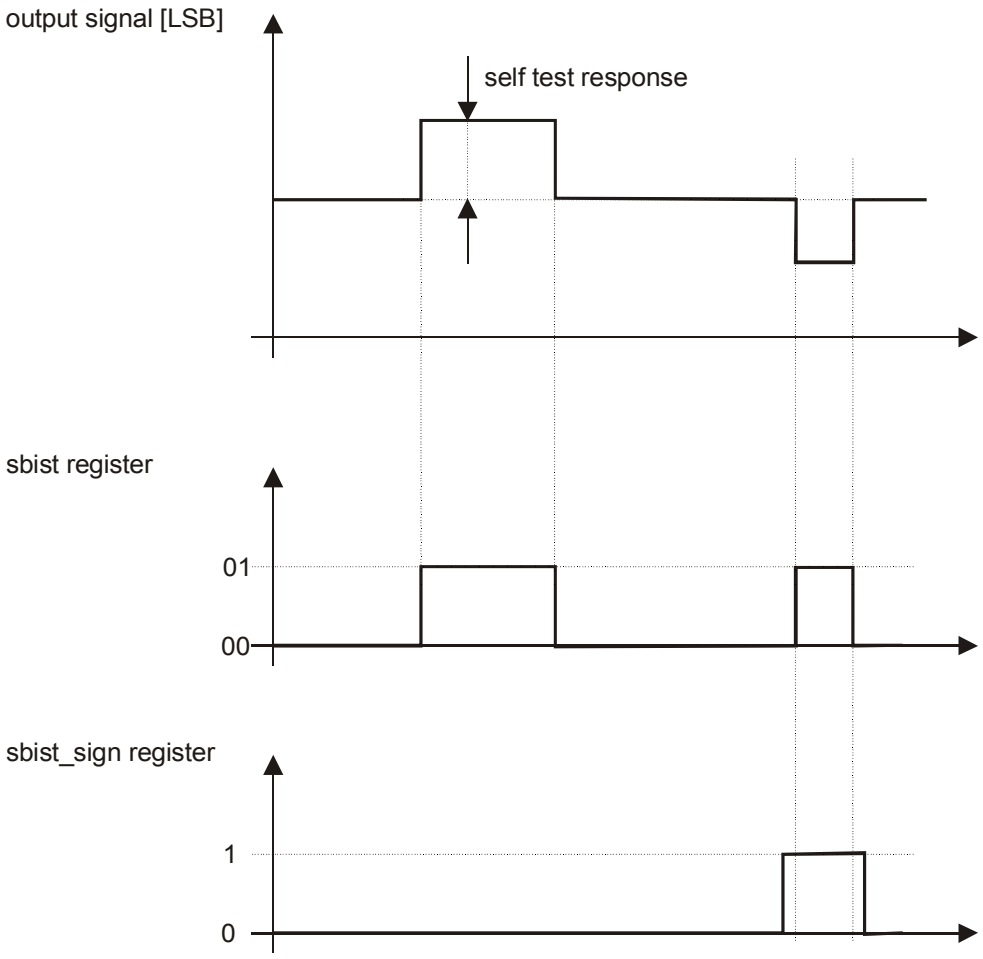
6.5 Self test mode

The sensor features an on-chip self-test mode. The self test is realized by a physical deflection of the seismic mass due to an applied electrostatic force. Thus, it provides full testing of the complete signal evaluation path including the micromachined sensor structure and the evaluation ASIC.

The self test mode can be activated individually for each axis by setting the the *sbist* register to the corresponding value ('01'=x-axis, '10'=y-axis, '11'=z-axis). The self test works in all acceleration ranges. By setting the *sbist_sign* register to '1', the polarity of the self test signal can be changed from positive to negative.

The self test response remains as a static offset on the output as long as the *sbist* register is not set back to '00'. While the self test is activated, any acceleration or gravitational force applied to the sensor will be observed in the output signal as a superposition of both acceleration and self test signal.

Figure 13: Self-test mode



7 Interfaces

The BMA220 can connect to the host system via three interfaces:

- SPI (3-wire, 4-wire)
- I²C
- Dedicated mode pins (for µC-less- or stand-alone operation, see section 0)

In SPI and I²C mode, the BMA220 supports two commands: **read** and **write**. The ASIC can be entirely controlled through those commands. A detailed register to address mapping can be found in section 0.

It should be noted that there is no way to access internal control or configuration registers while the BMA220 is in one of its dedicated modes.

In I²C and SPI mode, the internal registers can be accessed via a 7-bit address. Each read- and write-cycle accesses 8 bits only.

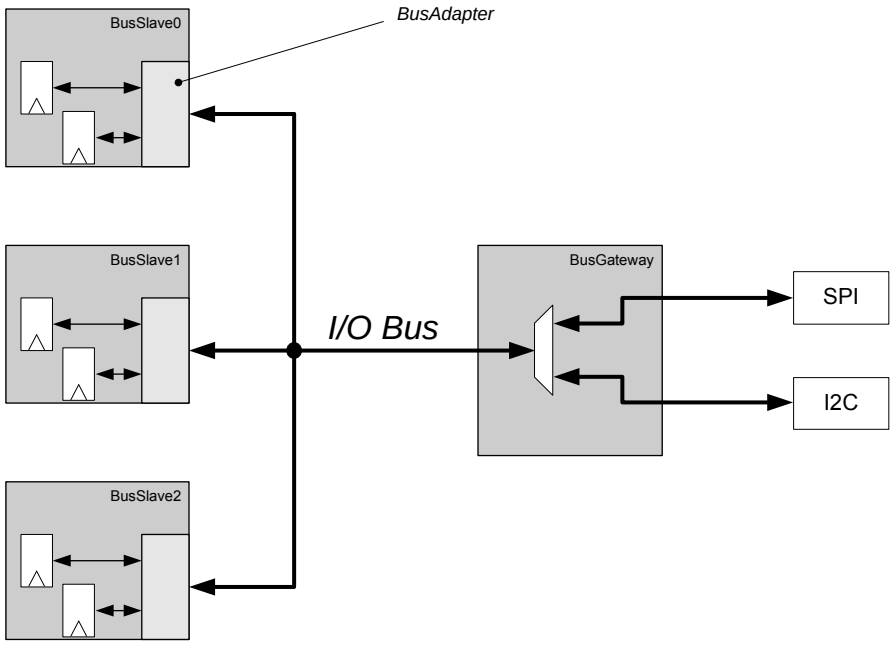


Figure 14: BMA220 I/O bus concept

The SPI and I²C interfaces are connected to the internal *bus gateway* which activates either one of the two interfaces according to the current mode. All internal digital modules accessible via the serial interfaces are called *bus slave*. Each slave is connected to the internal bus through a *bus adapter*.

7.1 General digital interface description

In general there are two common digital protocols selectable, the serial interfaces I²C and SPI. By default, SPI is used in the standard 4-wire configuration. The SPI interface may be configured by SW to operate in 3-wire interface mode, instead of standard 4-wire mode.

The two serial interfaces are mapped onto the same pads. An external pin is needed to switch between the interfaces. When this protocol select pin (PS) is connected to VSS, SPI is selected as the current interface; when the select pin is connected to VDDD, I²C is used as the interface. When select pin is left floating, one of the dedicated modes is selected.
The BMA220 doesn't provide a functional analog output of the three axes since there is just CAP0 available in the package.

PIN Name	PIN description
CSB	SPI serial enable bar
SCK/SCL	SPI serial clock (SCK) I²C serial clock (SCL)
SDI/SDO/SDA	SPI serial data input (SDI) SPI serial data output in 3-wire SPI mode (SDO) I²C serial data (SDA)
SDO	SPI serial data output

Table 19: Interface pin name

7.2 SPI interface

The SPI interface integrated in BMA220 is a slave SPI. 16-bit protocols are used for single byte reading and writing. Multiple bytes read-out is also possible. However, multiple bytes write is not supported.
4-wire SPI and 3-wire SPI are using same protocols. The communication starts with a read/write control bit followed by 7 bits address and at least 8 bits data. In case of reading out of acceleration data from all axes the chip provides the option to use an automatic incremented read command to read more than one byte (multiple read). This is activated when the SPI serial enable pin CSB is held low during the data readout. Thus data from next address will be automatically read out if the CSB are kept low for another 8 SPI clock cycles.

4-wire SPI protocol and timing
4-wire SPI is the default serial interface. It interacts with the outside world using CSB (chip select low active), SCK (serial clock), SDI (serial data input) and SDO (serial data output).
The communication starts when the CSB is pulled low by the SPI master and stops when CSB is pulled high. SCK is also controlled by SPI master. During the transitions on CSB, SCK must be high. SDI and SDO are driven at the falling edge of SCK and should be captured at the rising edge of SCK.
Single byte write/read commands use 16-bits protocol.

Bit0: Read/Write bit. When 0, the data SDI is written into the chip. When 1, the data SDO from the chip is read.

Bit1-7: Address AD(6:0).
Bit8-15: when in write mode, these are data SDI, which will be written into the address. When in read mode, these are the data SDO, which are read from the address.

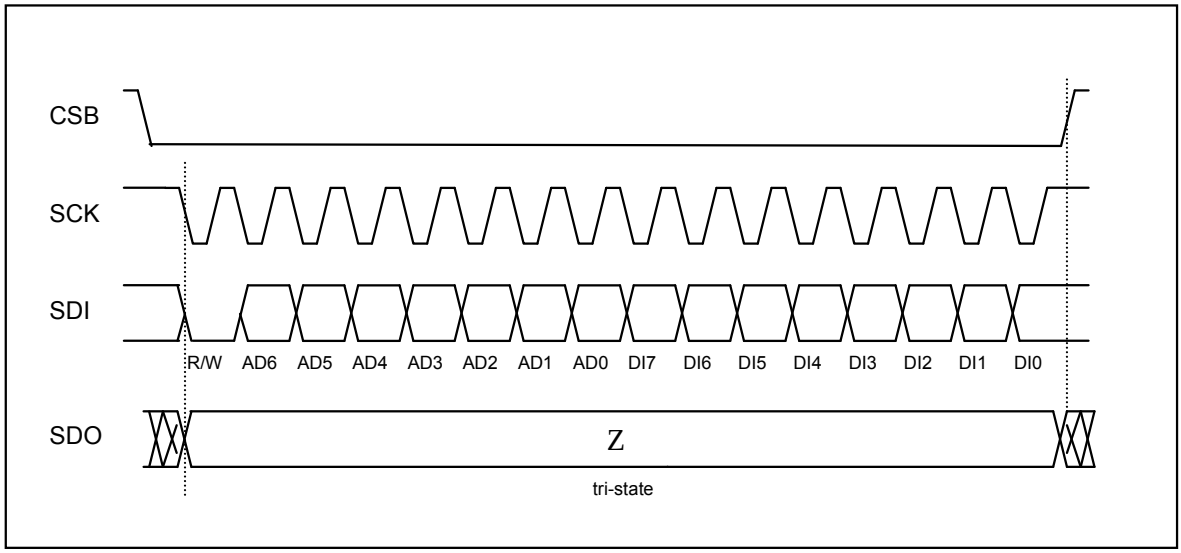


Figure 15: 4-wire SPI write command

Write command is completed in 16 clock cycles. During the entire write cycle SDO remains in high- impedance state.

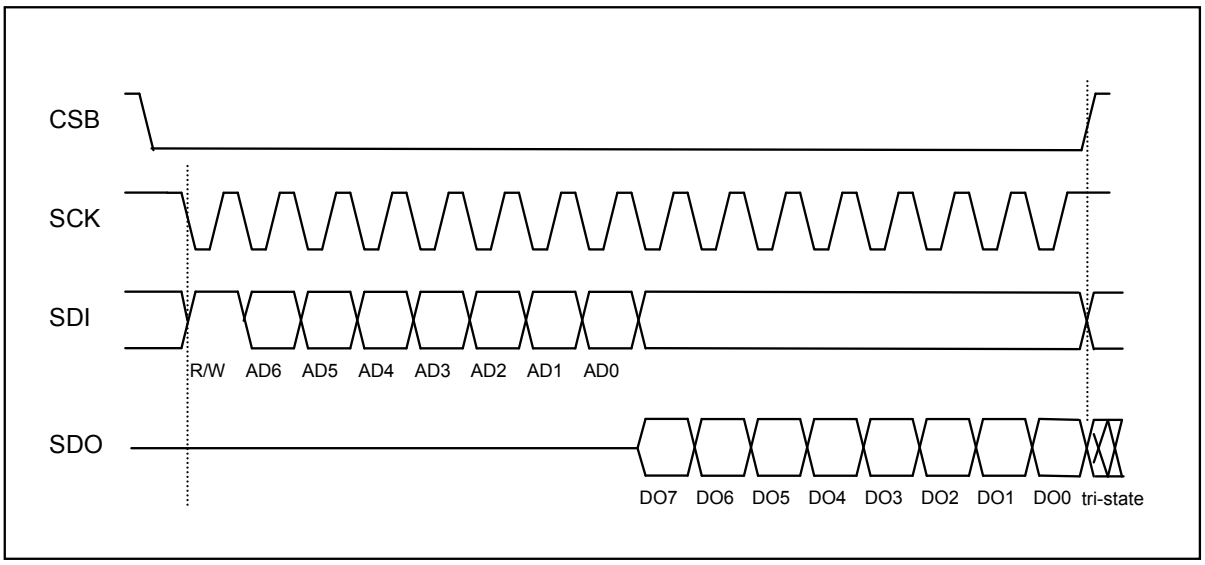


Figure 16: 4-wire SPI read command

Read command is completed in 16 clock cycles or in multiple of 8 in case of multiple byte read. In multiple-read cycle further blocks of 8 clock periods will be extended for each acknowledged data.

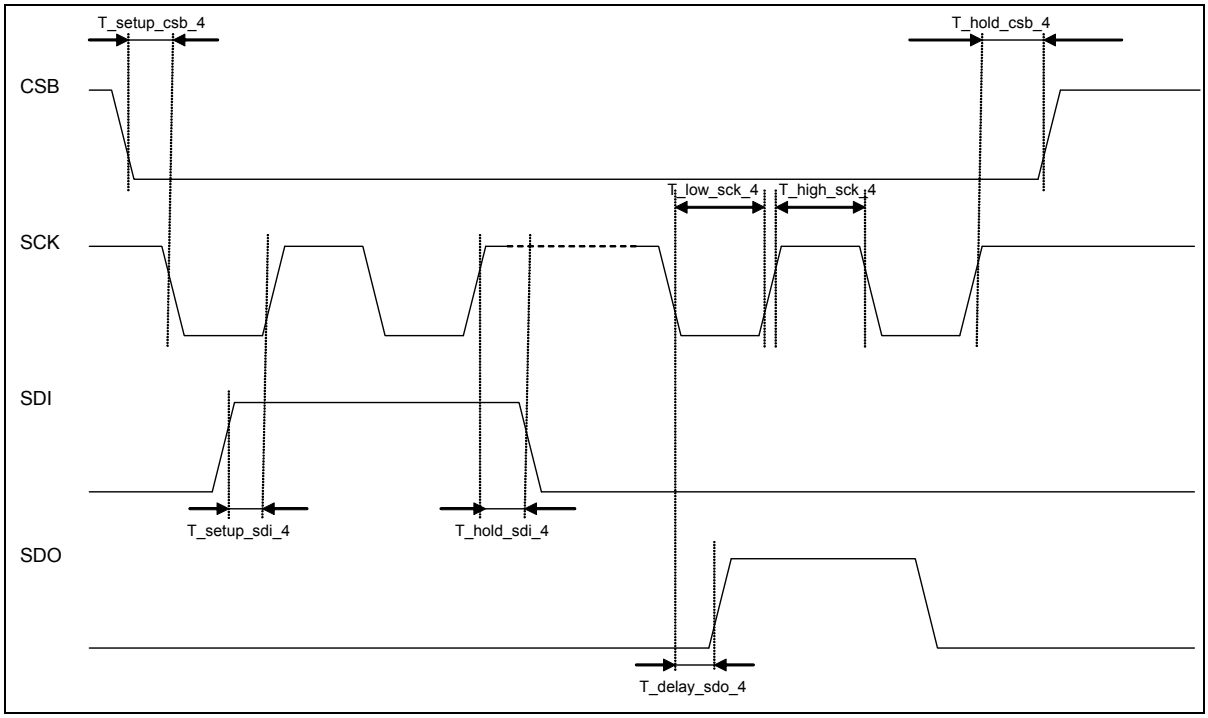


Figure 17: Timing diagram of 4-wire SPI cycle

Parameter	Symbol	Condition	Min	Units
CSB lead time	T_setup_csb		10	ns
CSB lag time	T_hold_csb		10	
SDI setup time	T_setup_sdi		5	
SDI hold time	T_hold_sdi		5	
SDO delay time	T_delay_sdo	C_{Load} ≤ 50pF	30 (MAX)	
SCK period	T_sck		100	

Table 20: SPI Timing

3-wire SPI

3-wire SPI interface uses SDI pin for both data input and output. It can be invoked by setting the SPI3 register bit at address 0x0F.

The write command for the 3-wire SPI is identical to the 4-wire SPI write command. When a read command is performed, output data are redirected to SDI pin after last address bit AD0 is latched. No extra clock cycle is needed for output redirection.
Output data are synchronized at falling edge of SCK. Both input and output data shall be captured at rising edge of SCK.

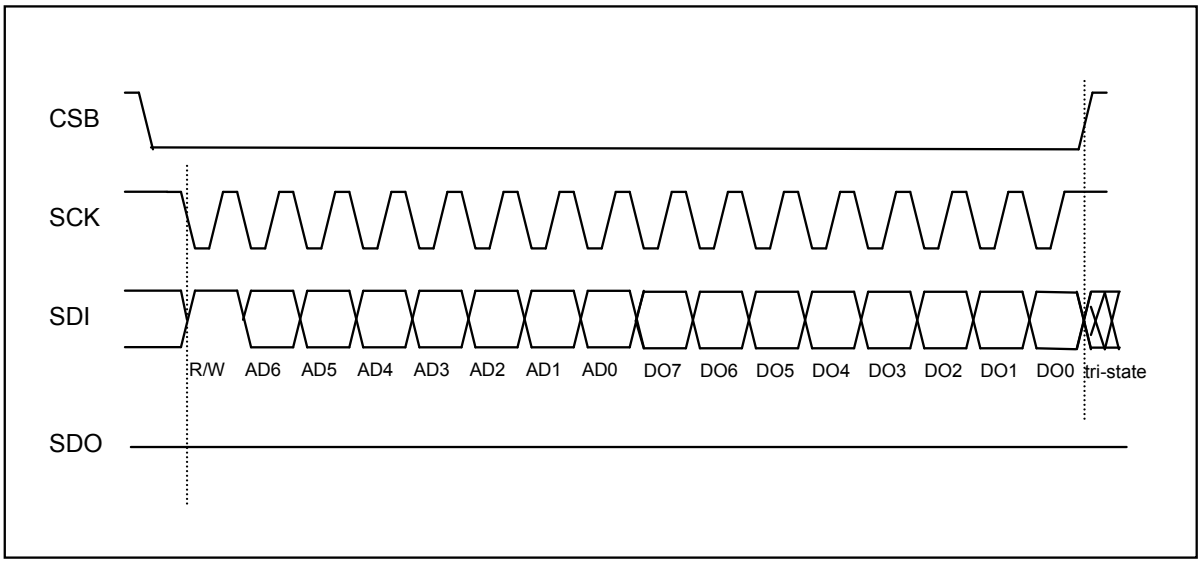


Figure 18: 3-wire SPI read protocol

7.3 I²C interface

The I²C interface on board is a slave bus. Two signal lines SCL and SDA are used for communication. SDA is a bidirectional line used for sending and receiving data to/from the interface. SCL is the serial clock line used to synchronize the data. Both lines are connected to VDD via pull-up resistors. So the lines are pulled high when the bus is free. The lines are low only when any of the transmitters drives '0'. The on-board I²C interface supports standard and fast-mode I²C.

Important:
The default slave address assigned to the BMA220 is *000 1011*. When in I²C mode, the LSB can be inverted by tying the CSB pin to '1'. This allows resolving conflicts with existing devices. Also, the 4 LSB can be configured via OTP.

I²C protocol:
Start and stop conditions (see Figure 19):
Data transmission on the bus begins with a HIGH to LOW transition on SDA line while SCK is held high (start condition (S) indicated by I²C bus master). Once the START signal is transferred by the master, the bus is considered busy.
Each data transfer should be terminated by a Stop signal (P) generated by master. The STOP condition is a LOW to HIGH transition on SDA line while SCK is held high.

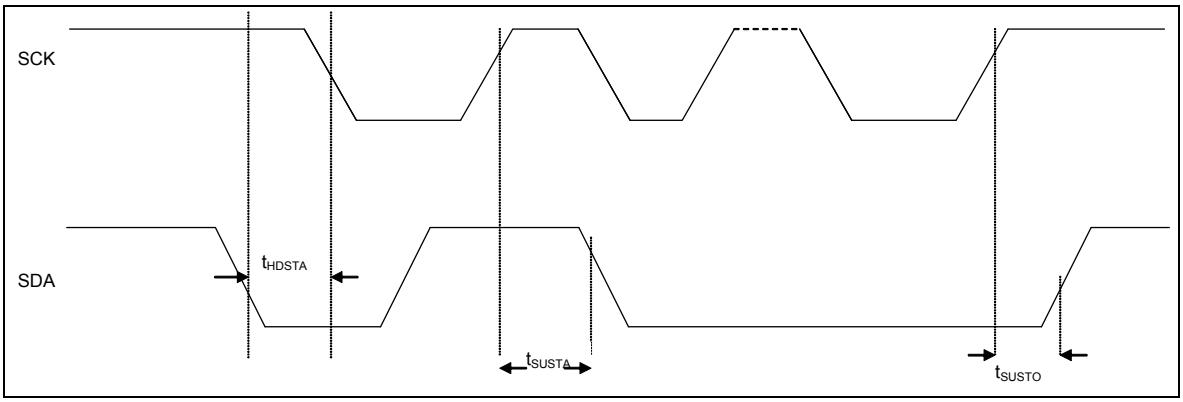


Figure 19: Waveform diagram for I²C start and stop conditions

Parameter	Symbol	Condition	Min	Units
START hold time	T_{HDSTA}		0.6	µs
START setup time	T_{SUSTA}		0.6	
STOP setup time	T_{SUSTO}		0.6	
Internal hold time	T_{HOLD_INT}	t_{f_SDA} = 100 ns t_{f_SCL} = 100 ns	0.3 (MAX)	
Clock to Data Out	T_{VD_ACK}	t_{f_SDA} = 100 ns t_{f_SCL} = 100 ns	0.08	

Table 21: I²C start/stop timing

Acknowledge:
Each byte of data transferred must be acknowledged. It is indicated by an acknowledge bit sent by the receiver. The transmitter must release the SDA line (no pull down) during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

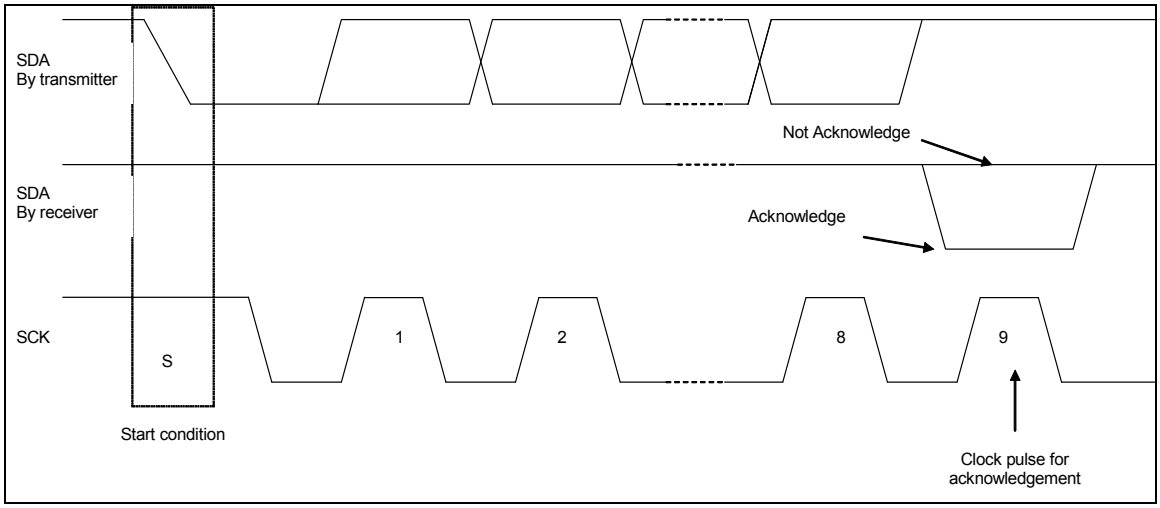


Figure 20: Waveform diagram for I²C acknowledgement on SDA

Data Transfer:
Each data bit transferred via SDA line must remain stable during high period of SCK pulse.

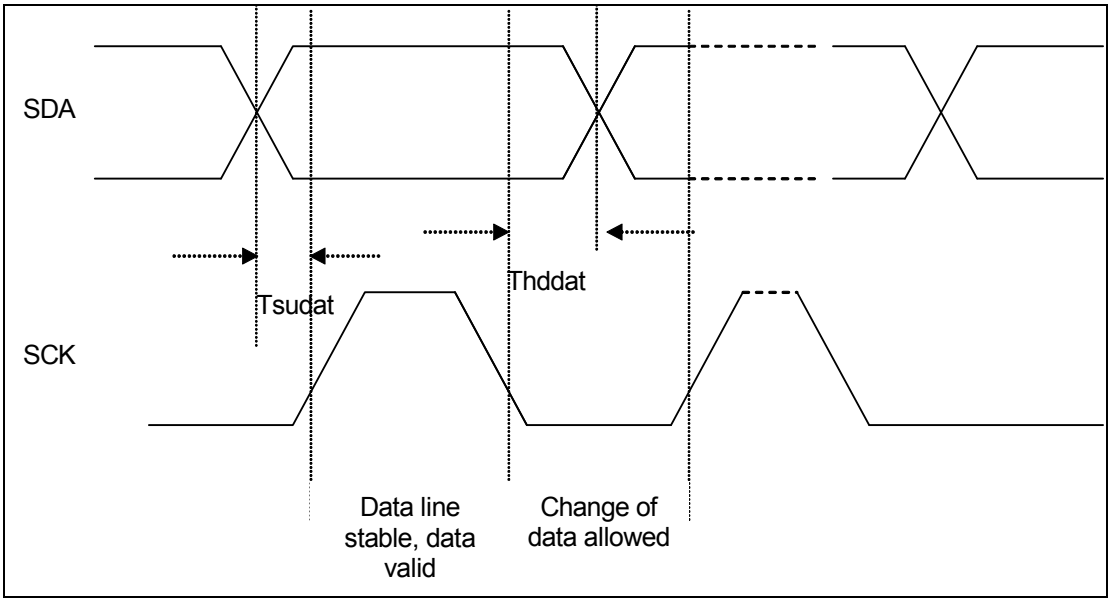


Figure 21: Waveform diagram for one bit transfer with I²C interface

#	Parameter	Symbol	Min	Max	Units
1	DATA hold time	T_{HDDAT}	0	0.9	µs
2	DATA setup time	T_{SUDAT}	0.1	-	

Table 22: I²C data transfer timing

The first byte of data transmitted after start condition contains the 7-bit address of I²C slave. The 8th bit is an R/W bit which tells whether the master wants to read (R/W = 1) or write (R/W = 0) data from/to the slave.
Once the slave is addressed, it sends a low active acknowledge bit and accepts the following data transferred by master. Otherwise it aborts the current data transfer and waits for the start condition of next data transmission.

I²C write command:
I²C write command only supports one byte writing. The protocol begins with start condition generated by master, followed by 7bits slave address and a write bit (R/W = 0). The slave sends an acknowledge bit (ACK = 0) and releases the bus. Then master sends the one byte register address (only the first 7bits are the valid address bits, the LSB shall be ignored). The slave shall again acknowledge the transmission and wait for the 8bits data which shall be written to the specified register address. After slave acknowledges the data byte, master generates a stop signal and terminates the writing protocol.
Data transferred by Master
Data transferred by Slave

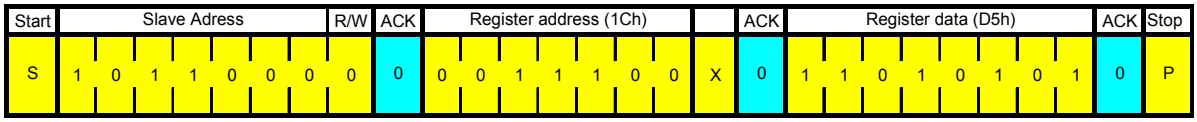


Figure 22: I²C one byte write protocol

I²C read command:

I²C read command supports multiple bytes reading. A read command consists of a 1-byte I²C write phase followed by I²C read phase. The two I²C transmissions must be separated by a repeated start condition (Sr). The I²C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, master generates again a start condition and sends the slave address together with a read bit (R/W = 1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK (ACK = 1) from master stops the data transferring from slave. Slave releases the bus so that master can generate a STOP condition and terminate the transmission.

Register address is automatically incremented and more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the latest I²C write command. By default the start address is set at 0x00. In this way repetitive multi-bytes reads from the same starting address are possible.

Data transferred by Master

Data transferred by Slave

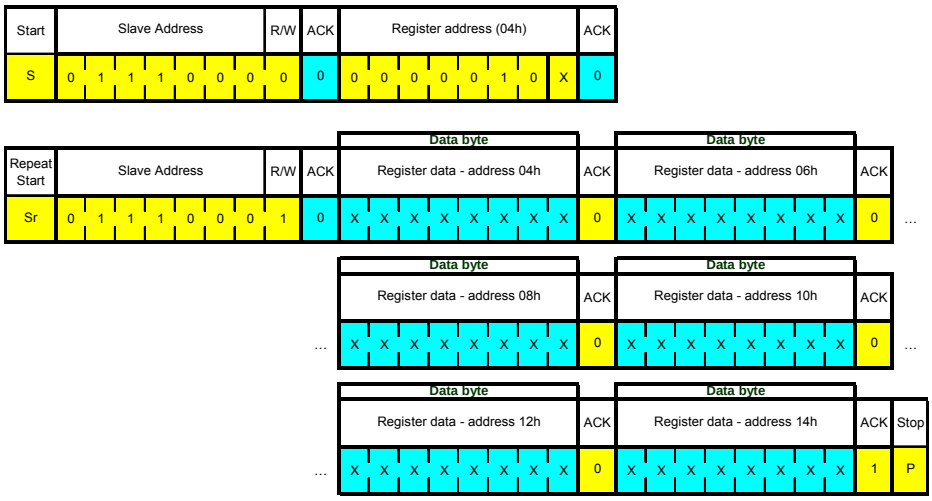


Figure 23: I²C multiple bytes read protocol

7.4 I²C watchdog timer

In order to prevent the built-in I²C slave to lock-up the I²C bus, a watchdog timer (WDT) is introduced. The WDT observes internal I²C signals and resets the I²C interface if the bus is locked-up by the BMA220.

The WDT observation period and WDT on/off can be configured through interface registers.

WDT_TO_en	WDT_TO_sel	WDT function
0	X	OFF
1	0	1 ms
1	1	10 ms

Table 23: WDT settings

7.5 SPI and I²C access restrictions

The required wait time after a write-cycle depends on whether the power-saving (sleep) mode is currently active. In case the low-power mode is active, the internal clock frequency is reduced and thus the required wait time increases.

Protocol	Access	Normal mode	Low-power mode
I^2C / SPI	Write	>3µsec	>300µsec
I^2C / SPI	Read	>2µsec	>2µsec

Table 24: Required wait times after write / before read access

X-after-Write

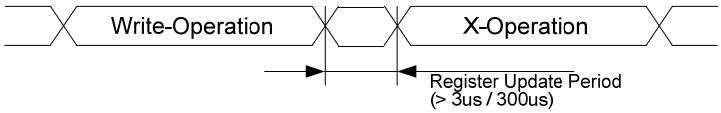


Figure 24: Post-Write access timing constraints

Read-after-X

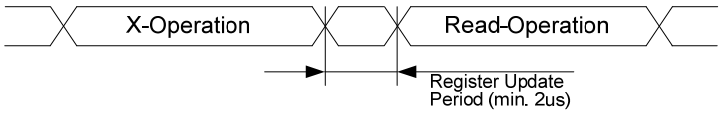


Figure 25: Pre-read access timing constraints

Please note that this read-constraint only applies to read-outs of the same axes. Reading out the three axes in a back-to-back transfer is possible!

8 Pin-out and connecting diagram

8.1 Pin-out

Figure 26: Pin-out of the BMA220 (top view)

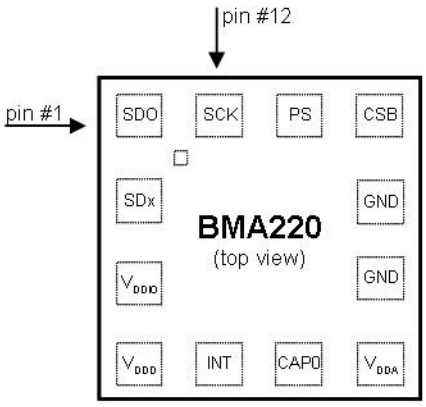


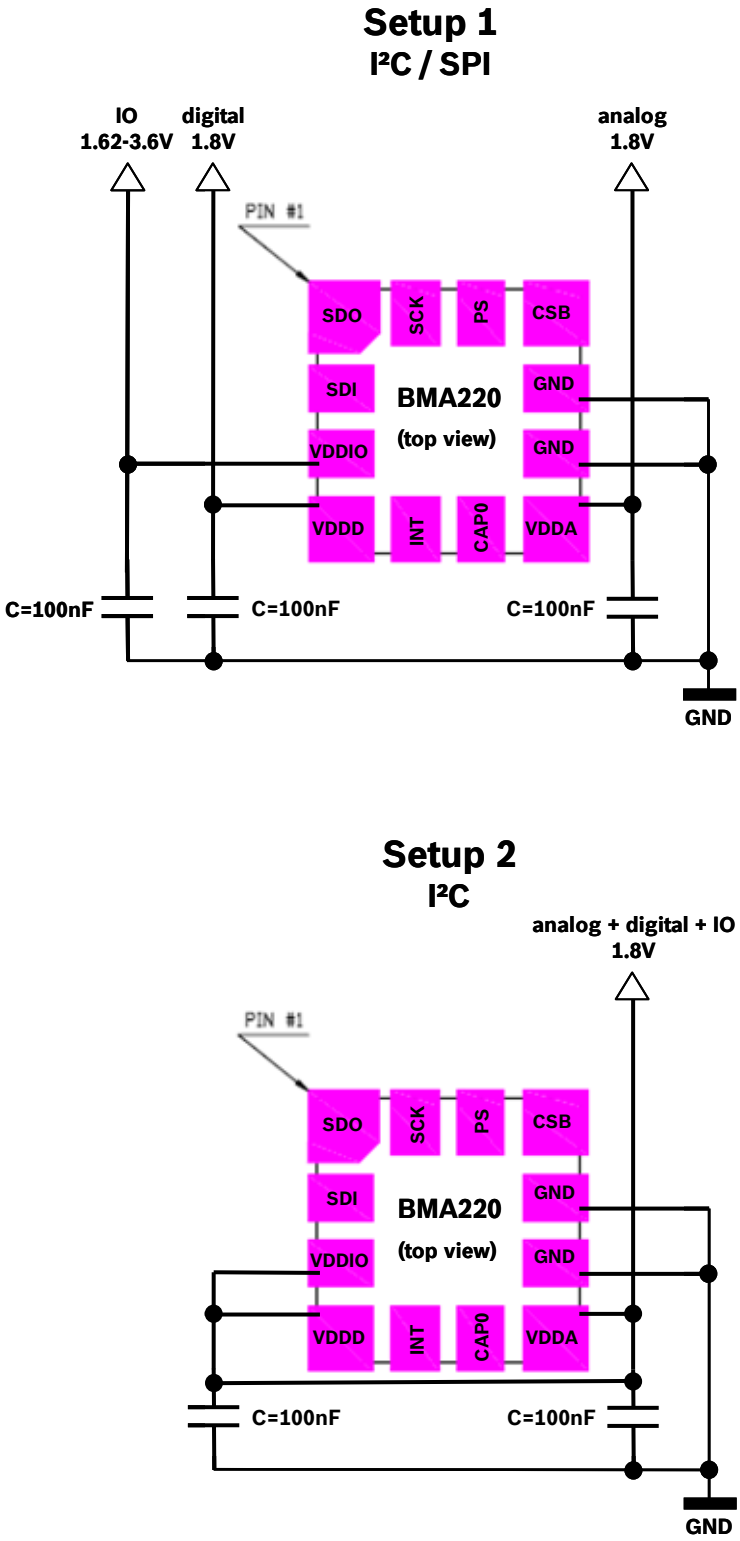
Table 25: Pin description

Pin#	Name	Type	Description	Connect to (in SPI 4w)	Connect to (in SPI 3w)	Connect to (in I²C)
1	SDO	Digital Out	SPI serial data output	SDO	NC	NC
2	SDx	Digital I/O	SDA for I^2C serial data in-/output SDI for serial data input (SPI 4-wire mode) SDA serial data in-/output (SPI 3-wire mode)	SDI	SDA	SDA
3	VDDIO	Supply I	I/O supply voltage (variable between 1.62 ... 3.6V)	VDDIO	VDDIO	VDDIO
4	VDDD	Supply I	Power supply for digital domain	VDDD	VDDD	VDDD
5	INT	Digital I/O	Interrupt output	INT	INT	INT
6	CAP0	DNC	Do not connect! Pin reserved for factory trimming	NC	NC	NC
7	VDDA	Supply I	Power supply for analog domain	VDDA	VDDA	VDDA
8	GND	Ground	Shared ground for digital, I/O and analog	GND	GND	GND
9	GND	Ground	Shared ground for digital, I/O and analog	GND	GND	GND
10	CSB	Digital In	Chip-select for SPI mode. Address-select for I^2C mode, see chapter 8.3. Pin must not float.	CSB	CSB	CSB
11	PS	Digital In	Protocol select pin (0=SPI, 1=I^2C, float = µC-less); pin must not float unless dedicated mode is used, see chapter 6.1.	GND	GND	VDDIO
12	SCK	Digital In	SCK for SPI serial clock SCL for I^2C serial clock	SCK	SCK	SCL

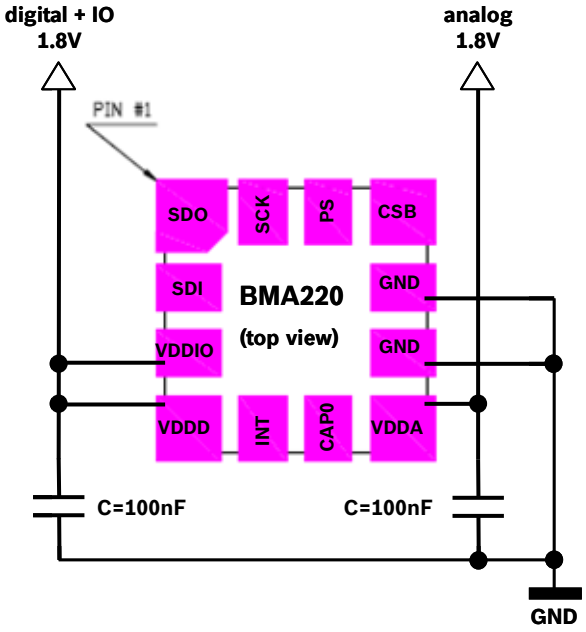
For further details on the recommended connection for the use of the BMA220 without µController (i.e. in dedicated I/O modes) please refer to table 16 in chapter 6.

8.2 Connecting diagrams

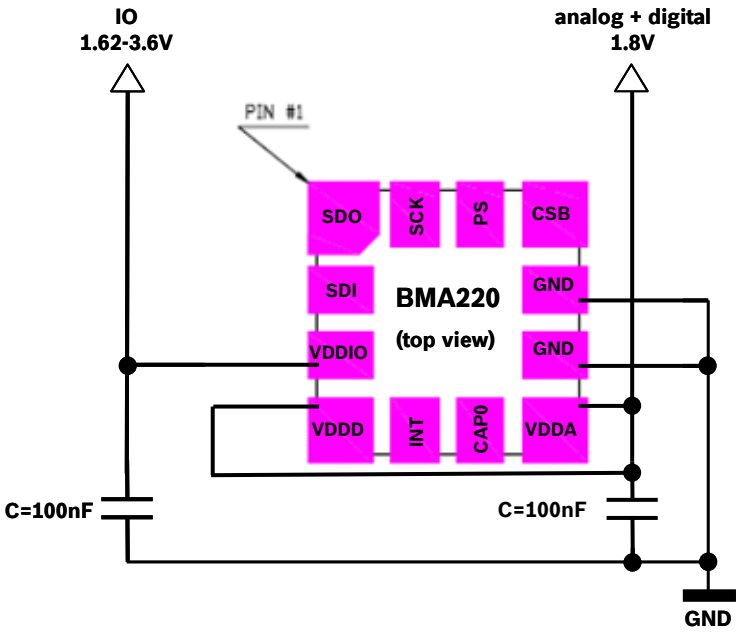
Figure 27: BMA220 electrical connecting diagram setup options



Setup 3
I²C / SPI



Setup 4
I²C / SPI



In order to prevent noise on the supply pins V_{DDA}, V_{DDD} and V_{DDIO} it is recommended to use low-leakage blocking capacitors with 100nF. The capacitors should be placed close to the respective pins as shown in figure 27.

V_{DDD}, V_{DDA} and V_{DDIO} can be connected according to the given diagrams, also to one common power supply within the specified range as long as the following requirement is met:

- For V_{DDA} the voltage noise level must not exceed 100mVpp for signals below 1kHz and must not exceed 10mVpp for signals above 1kHz.

In case SPI communication is used, it is recommended to apply a connection in accordance with diagrams as shown in setup 1, setup 3 or setup 4.

9 Package

9.1 Outline dimensions

The sensor housing is a standard LGA package. It is compliant with JEDEC Standard MO-229 Type VGGD-3. Its dimensions are the following.

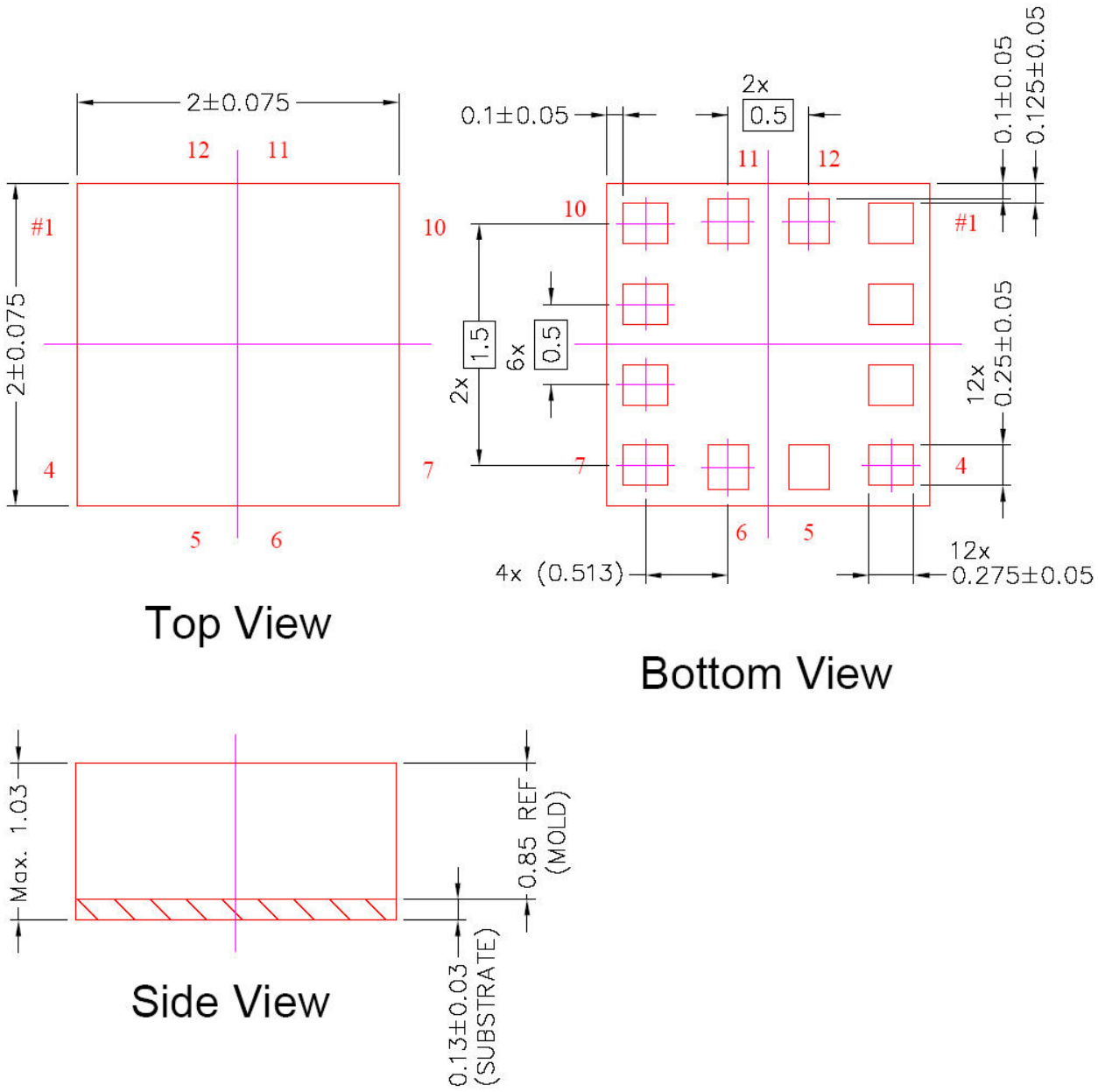


Figure 28: Outline dimensions (in mm)

9.2 Sensing axes orientation and polarity of the acceleration output

If the sensor is accelerated in the indicated directions, the corresponding channel will deliver a positive acceleration signal (dynamic acceleration). If the sensor is at rest and the force of gravity is working along the indicated directions, the output of the corresponding channel will be negative (static acceleration).

Example: If the sensor is at rest or at uniform motion in a gravity field according to the figure given below, the output signals are:

- ± 0g for the X channel
- ± 0g for the Y channel
- + 1g for the Z channel

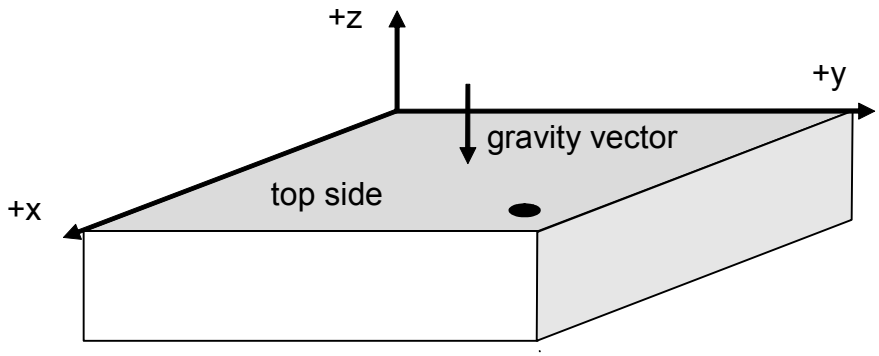


Figure 29: Orientation of sensing axes

The following table lists all corresponding output signals on X, Y, and Z while the sensor is at rest or at uniform motion in a gravity field under assumption of a ±2g range setting and a top down gravity vector as shown above.

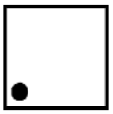
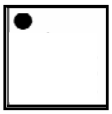
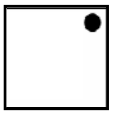
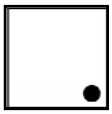
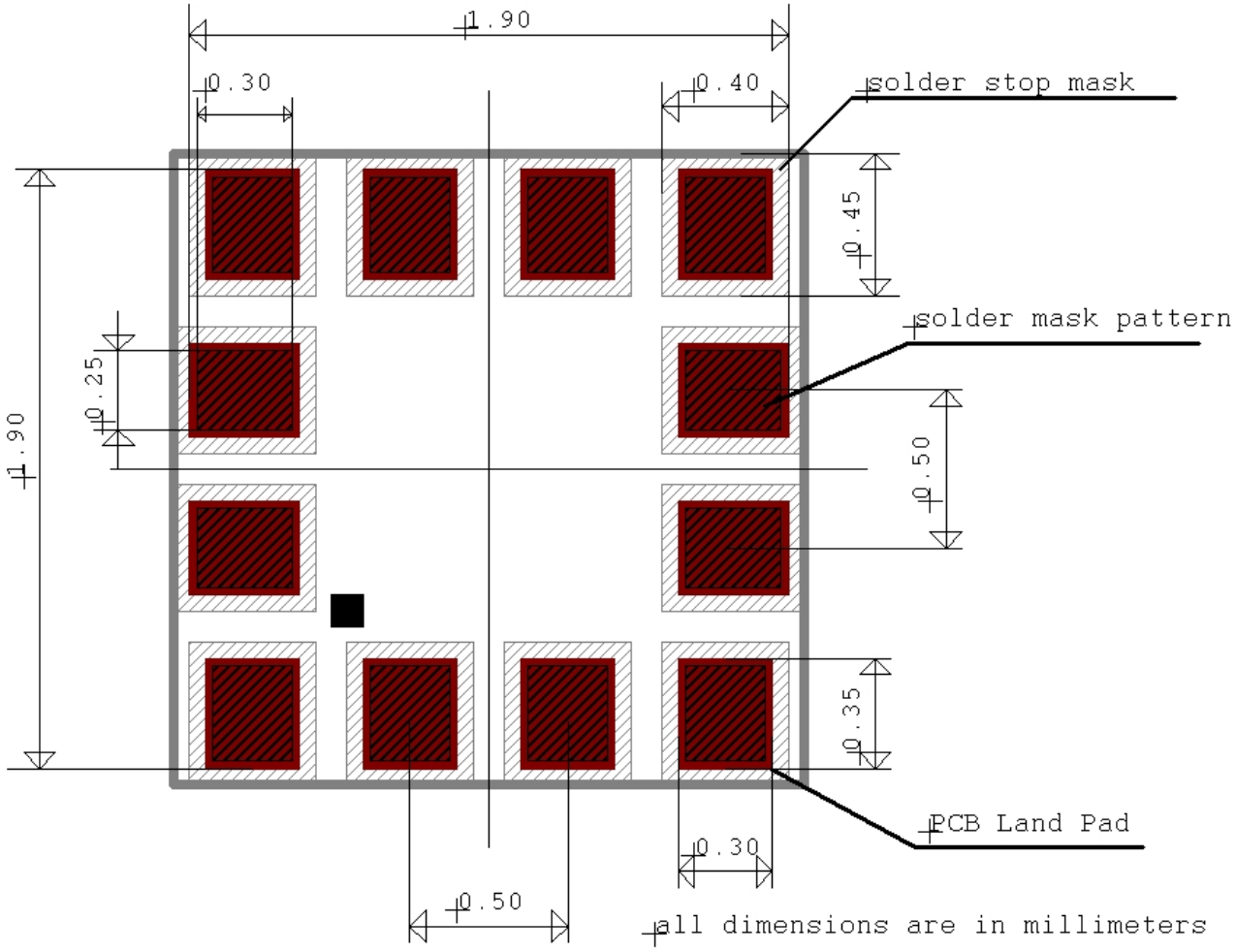
Sensor Orientation (gravity vector ↓)						
Output Signal X	0g / 0LSB	1g/16LSB	0g / 0LSB	-1g/-16LSB	0g / 0LSB	0g / 0LSB
Output Signal Y	-1g/-16LSB	0g / 0LSB	+1g / 1.8V	0g / 0LSB	0g / 0LSB	0g / 0LSB
Output Signal Z	0g / 0LSB	0g / 0LSB	0g / 0LSB	0g / 0LSB	1g/16LSB	-1g/-16LSB

Table 26: Output signals depending on sensor orientation

9.3 Landing pattern recommendation

As for the design of the landing patterns, the following recommendations can be given:

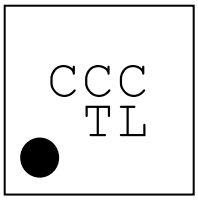
Figure 30: Landing patterns relative to the device pins, dimensions are in mm



9.4 Marking

9.4.1 Mass production samples

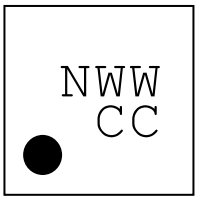
Figure 31: Marking of mass production samples



Labeling	Name	Symbol	Remark
	Lot counter	CCC	
	Product number	T	T = 1
	Sub-con ID	L	1 digit alphanumerical, code to identify sub-con and plant , L = A or L = U or L = P
	Pin 1 identifier	●	

9.4.2 Engineering samples

Figure 32: Marking of engineering samples



Labeling	Name	Symbol	Remark
	Eng. sample ID	N	Engineering Samples are always marked with N = “e”
	Date code	WW	calendar week
	Lot counter	CC	e.g. Eng. marking F1, F2 ... C1, C2
	Pin 1 identifier	●	

9.5 Moisture sensitivity level and soldering

The moisture sensitivity level of the BMA220 sensors corresponds to JEDEC Level 1, see also

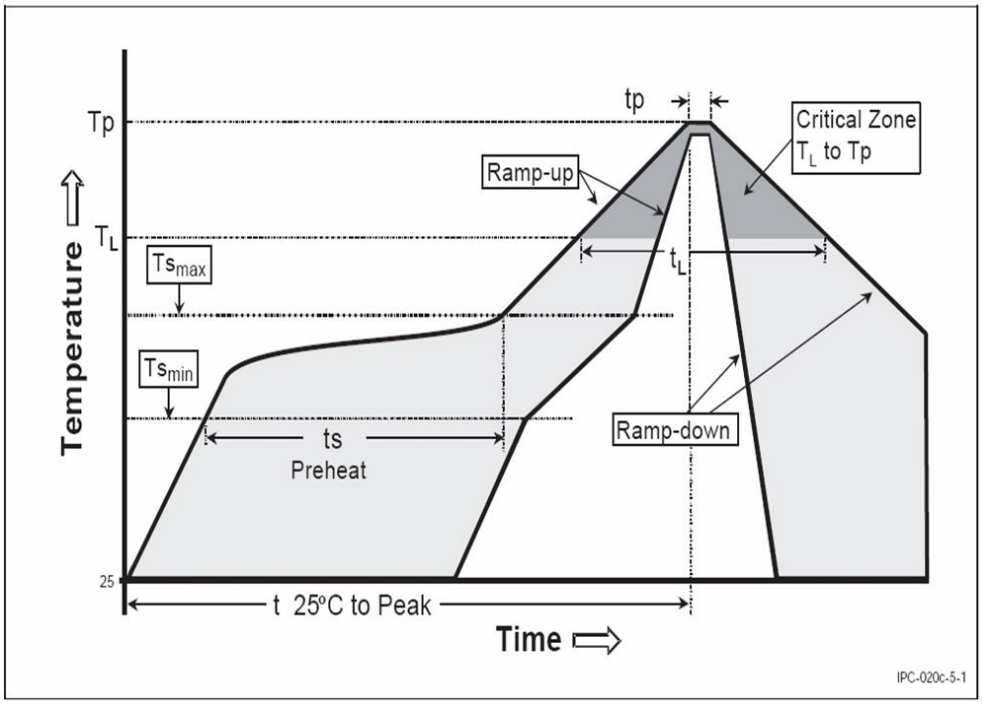
- IPC/JEDEC J-STD-020C "Joint Industry Standard: Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"

- IPC/JEDEC J-STD-033A "Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices".

The sensor fulfils the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, i.e. reflow soldering with a peak temperature up to 260°C.

Profile Feature		Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)		3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})		150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)		217 °C 60-150 seconds
Peak/Classification Temperature (Tp)		260 °C
Time within 5 °C of actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6 °C/second max.
Time 25 °C to Peak Temperature		8 minutes max.

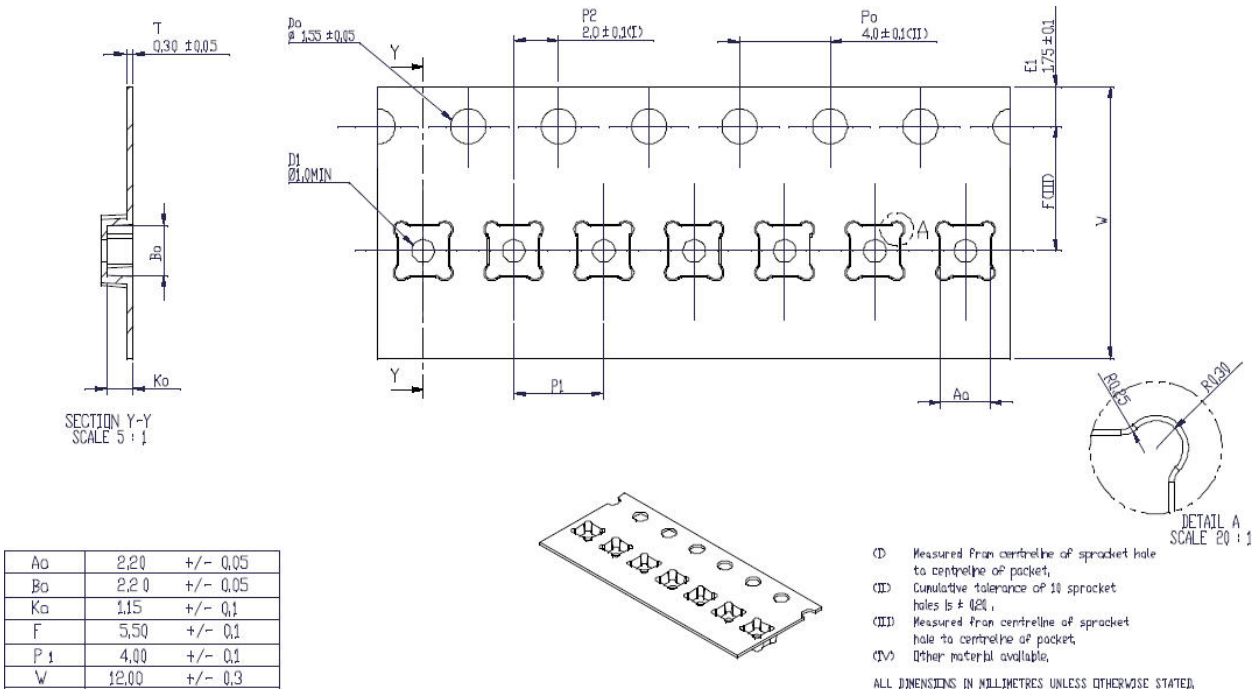
Note 1: All temperatures refer to topside of the package, measured on the package body surface.



9.6 Tape and reel specification

The BMA220 is shipped in a standard cardboard box.
The box dimension for 1 reel is: L x W x H = 35cm x 35cm x 6cm
BMA220 quantity: 10,000pcs per reel, please handle with care.

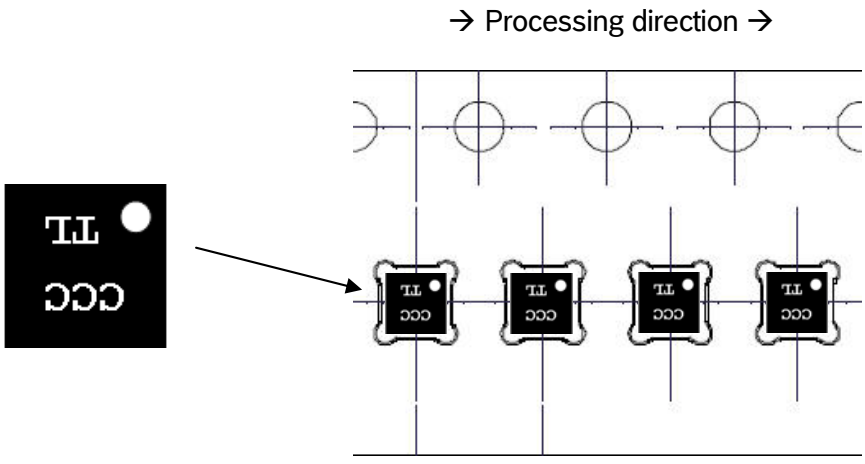
Figure 33: reel dimensions in mm



Ao	2,20	+/- 0,05
Bo	2,20	+/- 0,05
Ko	1,15	+/- 0,1
F	5,50	+/- 0,1
P1	4,00	+/- 0,1
W	12,00	+/- 0,3

9.7 Orientation

Figure 34 shows the orientation of the BMA220 devices relative to the tape.



9.8 RoHS compliancy

The BMA220 sensor meets the requirements of the EC restriction of hazardous substances (RoHS) directive, see also:

Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

9.9 Halogen content

Results of chemical analysis indicate that the BMA220 contains less than 900ppm (by weight) of Fluorine, Chlorine, Iodine and Bromine (i.e. < 50ppm per each substance). Therefore the BMA220 can be regarded as halogen-free. For more details on the analysis results please contact your Bosch Sensortec representative.

9.10 Note on internal package structure

Within the scope of Bosch Sensortec's ambition to improve its products and secure the product supply while mass production, Bosch Sensortec qualifies additional sources for the LGA package of the BMA220.

While Bosch Sensortec took care that all of the technical packages parameters are described above are 100% identical for both sources, there can be differences in the chemical content and the internal structural between the different package sources.

However, as secured by the extensive product qualification process of Bosch Sensortec, this has no impact to the usage or to the quality of the BMA220 product.

9.11 Handling instruction

Micromechanical sensors are designed to sense acceleration with high accuracy even at low amplitudes and contain highly sensitive structures inside the sensor element. The MEMS sensor can tolerate mechanical shocks up to several thousand g's. However, these limits might be exceeded in conditions with extreme shock loads such as e.g. hammer blow on or next to the sensor, dropping of the sensor onto hard surfaces etc.

We recommend to avoid g-forces beyond the specified limits during transport, handling and mounting of the sensors in a defined and qualified installation process.

This device has built-in protections against high electrostatic discharges or electric fields (2kV HBM); however, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

10 Legal disclaimer

10.1 Engineering samples

Engineering Samples are marked with an “e”. Samples may vary from the valid technical specifications of the product series contained in this data sheet. They are therefore not intended or fit for resale to third parties or for use in end products. Their sole purpose is internal client testing. The testing of an engineering sample may in no way replace the testing of a product series. Bosch Sensortec assumes no liability for the use of engineering samples. The Purchaser shall indemnify Bosch Sensortec from all claims arising from the use of engineering samples.

10.2 Product use

Bosch Sensortec products are developed for the consumer goods industry. They may only be used within the parameters of this product data sheet. They are not fit for use in life-sustaining or security sensitive systems. Security sensitive systems are those for which a malfunction is expected to lead to bodily harm or significant property damage. In addition, they are not fit for use in products which interact with motor vehicle systems.

The resale and/or use of products are at the purchaser’s own risk and his own responsibility. The examination of fitness for the intended use is the sole responsibility of the Purchaser.

The purchaser shall indemnify Bosch Sensortec from all third party claims arising from any product use not covered by the parameters of this product data sheet or not approved by Bosch Sensortec and reimburse Bosch Sensortec for all costs in connection with such claims.

The purchaser must monitor the market for the purchased products, particularly with regard to product safety, and inform Bosch Sensortec without delay of all security relevant incidents.

10.3 Application examples and hints

With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Bosch Sensortec hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights or copyrights of any third party. The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. They are provided for illustrative purposes only and no evaluation regarding infringement of intellectual property rights or copyrights or regarding functionality, performance or error has been made.

11 Document history and modification

Rev.	Chapter	Description of modification/changes	Date
0.9	All	Document creation	01-Dec-2008
0.91	All	Total document update	20-Aug-2009
0.92	1	Introduced resolution in table 1	20-Oct-2009
	2	Updated and extended table 2	
	9.1	Changed “VSS” to “GND”	
	9.2	Changes recommended capacitor for V_{DDA} to 100nF	
	9.2	Added recommendation, modified fig. 28	
	10.6	Updated quantity per reel	
0.93	1	Introduced resolution, current + timings in table 1	21-Dec-2009
	2	Updated and extended table 2	
	4	Updated global memory map incl. note	
	4.1.5	Updated soft-reset description	
	4.1.6	Updated suspend description	
	5.5	Updated table 10	
	6	New table 16	
	6.3.	Introduced current consumption estimation in low power mode	
	7	Removed	
	ex 8.3 new 7.3	Updated I^2C in fig. 23	
	ex 8.5 new 7.5	New table	
	ex 9.1 new 8.1	Changed “VSS” to “GND”, introduced “not float” indication	
		New table 25	
	ex 9.2 new 8.2	Changes recommended capacitor for V_{DDA} to 100nF	
	ex 9.2 new 8.2	Added recommendation, modified fig. 27	
	ex 10.6 new 9.6	Updated quantity per reel + figures	
	ex 10.8 new 9.8	Added < 50ppm each substances	
1.00	1	Clarified names of operation modes, introduced voltage input and output levels updated TCO, TCS, noise, temperature range, cross axis sensitivity and self test response in table 1	14-Apr-2010
	4	Introduced default content in global memory map	
	4.1.2	Update chapter name / wordings	
	4.1.3	Update chapter name / wordings	
	6.3	Update chapter name / wordings	
	7.2	Update of tables 20 and 21	
	All	Changed naming from “sleep mode” to “low-power mode”	
1.01	Title	Changed technical reference codes	28 May 2010

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